BAT32A6300 Datasheet

Ultra-low-power 32-bit SoC microcontroller based on the ARM® Cortex®-M0+

Built-in 32K-byte Flash, integrated LDO, dedicated SoC for LIN transceivers

V0.5.5

Feature

- **Ultra-low-power operation environment:**
  - Supply voltage range: 5.5V~28V
  - Temperature range: -40℃ to 125℃
  - Low power modes: sleep mode, deep sleep mode
  - Operating power consumption: 80uA/MHz@64MHz
  - Power consumption in deep sleep mode: 42uA (MCU sleeps, LDO maintains 5V output)
- **Core:**
  - ARM®32-bitCortex®-M0+ CPU
  - Operation frequency: 32KHz~64MHz
- **Memory:**
  - 32KB Flash memory, shared program and data storage
  - 4KB SRAM memory with parity check
- **Power and reset management**
  - Built-in power-on reset (POR) circuit
  - Built-in voltage detection (LVD) circuit (threshold voltage settable)
- **Clock management:**
  - Built-in high-speed oscillator with accuracy (±1%). 1MHz~64MHz system clocks are available.
  - Built-in 15KHz low-speed oscillator
  - Support 1MHz~20MHz external crystal oscillator
- **Multiplier/divider module:**
  - Multiplier: support single-cycle 32-bit multiplication operations
  - Divider: support 32-bit signed integer division operations, only 4 or 8 CPU clock cycles to complete an operation
- **Enhanced DMA controller:**
  - Interrupt trigger start
  - Selectable transfer modes (normal transfer mode, repeat transfer mode, block transfer mode and chain transfer mode)
  - Transfer source/destination realm are selectable from the full address space range
- **Linkage controller:**
  - It can link event signals together to realize the linkage of peripheral functions
  - There are 20 types of event input and 9 types of event triggering
- **Rich analog peripherals:**
  - 12-bit ADC converter with 1.42Msps conversion rate, 10 external analog channels with temperature sensor(s) supporting for single-Comparator (CMP), built-in 2-channel comparator, selectable input source, reference voltage can be selected from 12-bit DAC output voltage or internal reference voltage (1.45V/2.4V can be selected)
  - Programmable gain amplifier (PGA), built-in 1-channel PGA with two external input pins, controlled time division multiplexing, programmable 1/2.5/4/8/10/16/32x gain, bias voltage: 1.45V, 2.4V, optional Vcap/2.
- **Input/output ports:**
  - I/O ports: 26
  - It can switch between N-channel open drain, TTL input buffering, and internal pull-up
  - Controller for built-in clock output/buzzer output
- **Serial two-wire debugger (SWD)**
- **Rich timers:**
  - 16-bit timer: 9 channels
  - Watchdog timer (WWDT): 1x
  - SysTick timer
- **Rich and flexible interfaces:**
  - 2 serial communication units: each unit can be freely configured as 1-channel standard UART, 1-channel SPI or 1-channel Simplified I^2C (UART0 of unit 0 supports software LIN communication)
  - LIN: 1 channel (Hardware support LIN2.2 protocol, compatible with LIN2.x protocol, also support SAEJ2602 protocol specification)
  - IrDA: 1 channel
  - Standard I^2C: 1 channel, support slave dual address
  - SPI: 1 channel
- **Integrated LIN transceiver, compliant with LIN 2.x/ SAE J2602 protocols**
- **Integrated 5V LDO, capable of supplying power to internal MCU and external devices, with input voltage range of 5.5 to 28V.**
- **Safety function:**
  - Comply with IEC/UL 60730 standards
  - Report abnormal storage access errors
  - Support RAM parity check
  - Support hardware CRC verification
  - Support important SFR protection to prevent misoperation
  - 128-bit unique ID number
  - Flash Level 2 protection in the debug mode (Level1: only perform flash full-scale erase, cannot be read or written. Level2: Emulator connection is invalid, can't operate on flash.)

channel conversion mode and multi-channel scan conversion mode. Conversion range: 0 to V_{REF} (1.45V/2.4V/Vcap are selectable)

- 12-bit D/A converter, 2-channel analog output, real-time output function, output voltage to internal comparator range: 0~V_{REF}, (V_{REF}=1.45V/2.4V/Vcap); output voltage to pins range: 0.3V~Vcap-0.3V

- **Package:**
  - QFN32

1 Overview

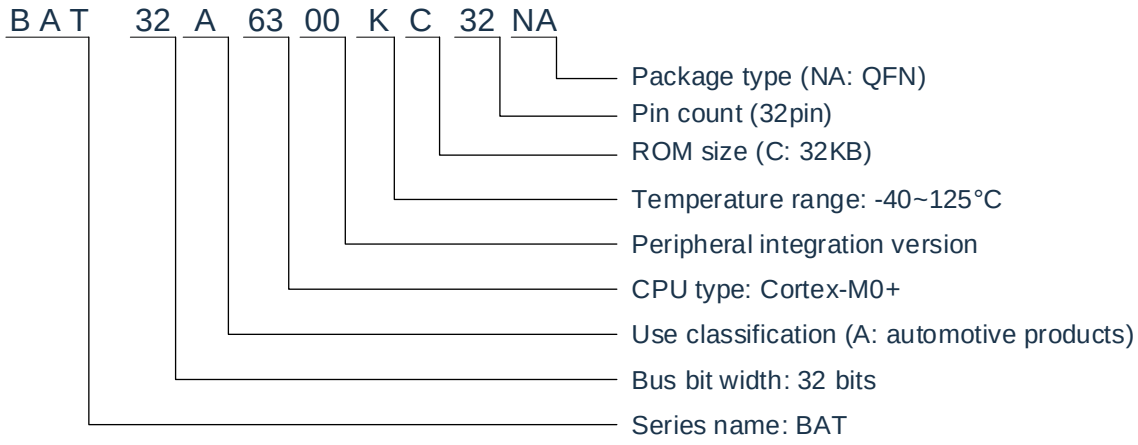
1.1 Brief introduction

BAT32A6300 series complies with AEC-Q100 Grade 1 automotive product standard, -40~125℃ operating temperature, supports 32Pin QFN package. This product adopts the high-performance ARM®Cortex®-M0+ 32-bit RISC core, which can operate up to 64MHz, and high-speed embedded flash memory (SRAM up to 4KB, program/data flash up to 32KB). The product integrates various standard interfaces such as I^2C, SPI, UART, LIN2.2 bus, 12-bit A/D converter, temperature sensor, 12-bit D/A converter, comparator, programmable gain amplifier. Integrated a variety of advanced timer modules, 1-channel SysTick timer, 9-channel 16-bit timer, watchdog timer and other functions, and integrated high-voltage LDOs, LIN transceivers and so on.

The BAT32A6300 also has excellent low-power performance, supporting both sleep and deep sleep modes for design flexibility. Its operating power consumption is 80uA/MHz@64MHz, and in deep sleep mode, its power consumption is only 42uA. At the same time, due to the integrated event linkage controller, direct connection between hardware modules can be realized without CPU intervention, which is faster than using interrupts.

The BAT32A6300 integrates LDO, LIN transceiver, and with excellent reliability, rich integrated peripheral functions, and outstanding low-power performance, it focuses on automotive electronics related to switches, doors, windows, lights, sensors, motors and other applications.

1.2 Product model list



Product list for BAT32A6300:

Product model	Flash memory	Dedicated data Flash memory	SRAM	Package
BAT32A6300KC32NA	32KB	-	4KB	32-pin plastic package QFN (5x5mm, 0.5mm pitch)

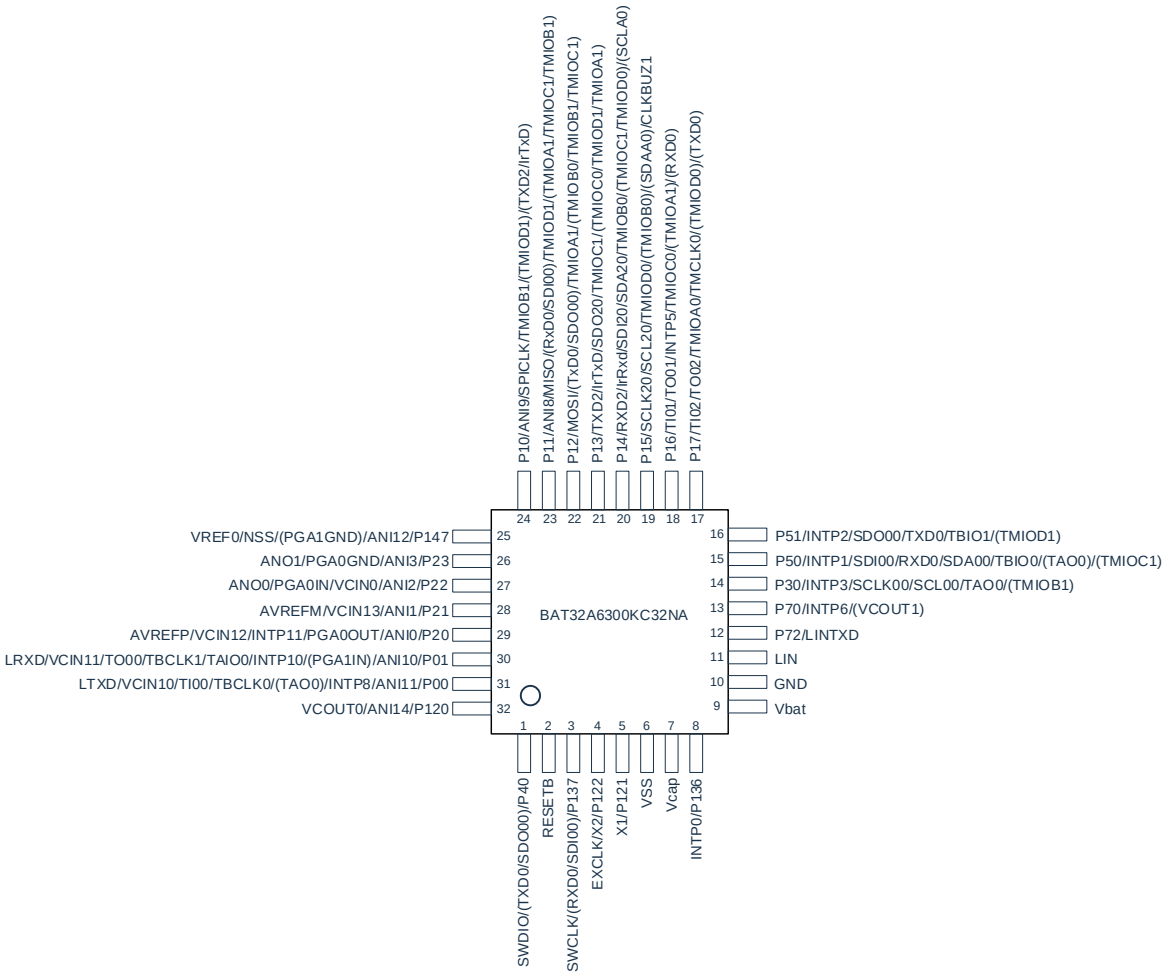
Product list for BAT32A6300:

Part No.	Core	Clock frequency (MHz)	Built-in LDO input (V)	MCU operating voltage (V)	Code Flash (KB)	SRAM (KB)	Data Flash (KB)	DMA	GPIO	12bit ADC	12t DAC	CMP	PGA	Universal timer (16bit)	Watchdog timer (WDT)	UART	SPI	IIC bus	LIN bus	CAN bus	Hardware multiplier	Hardware divider	Package
BAT32A6300KC32NA	M0+	64	5.5~28V	5.0	32	4	-	Y	26	10	2	2	1	9	1	2	1	1	1	-	Y	Y	QFN32

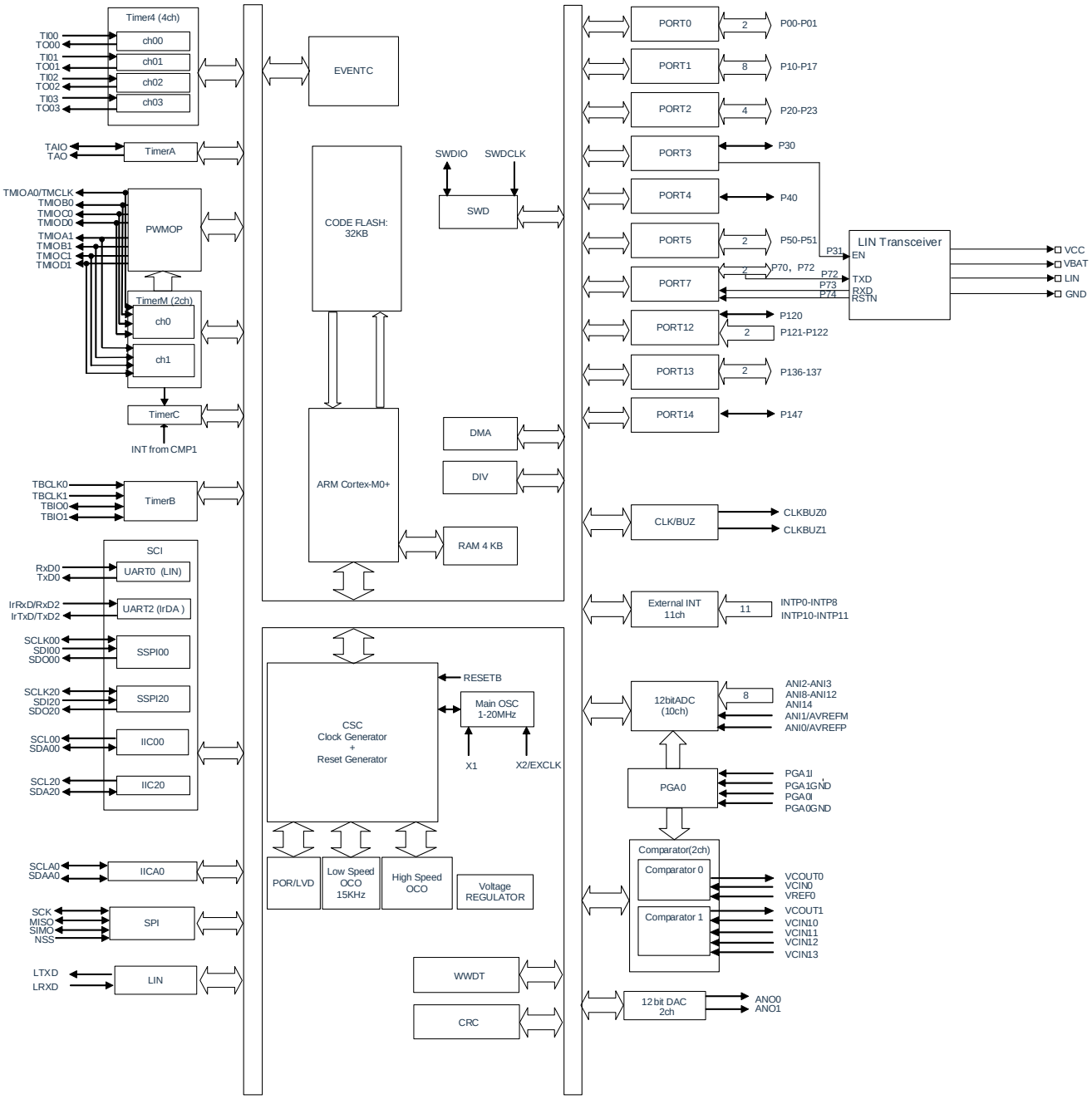
1.3 Top view

1.3.1 BAT32A6300KC32NA

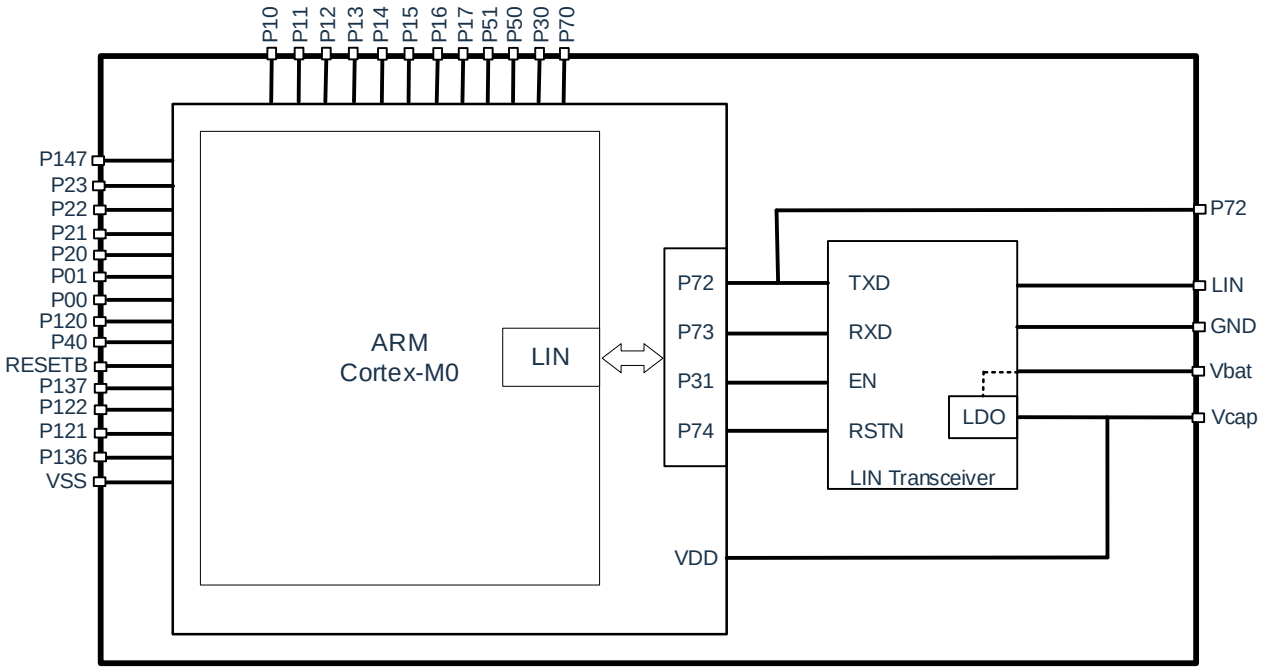
- 32-pin plastic QFN (5x5mm, 0.5mm pitch)



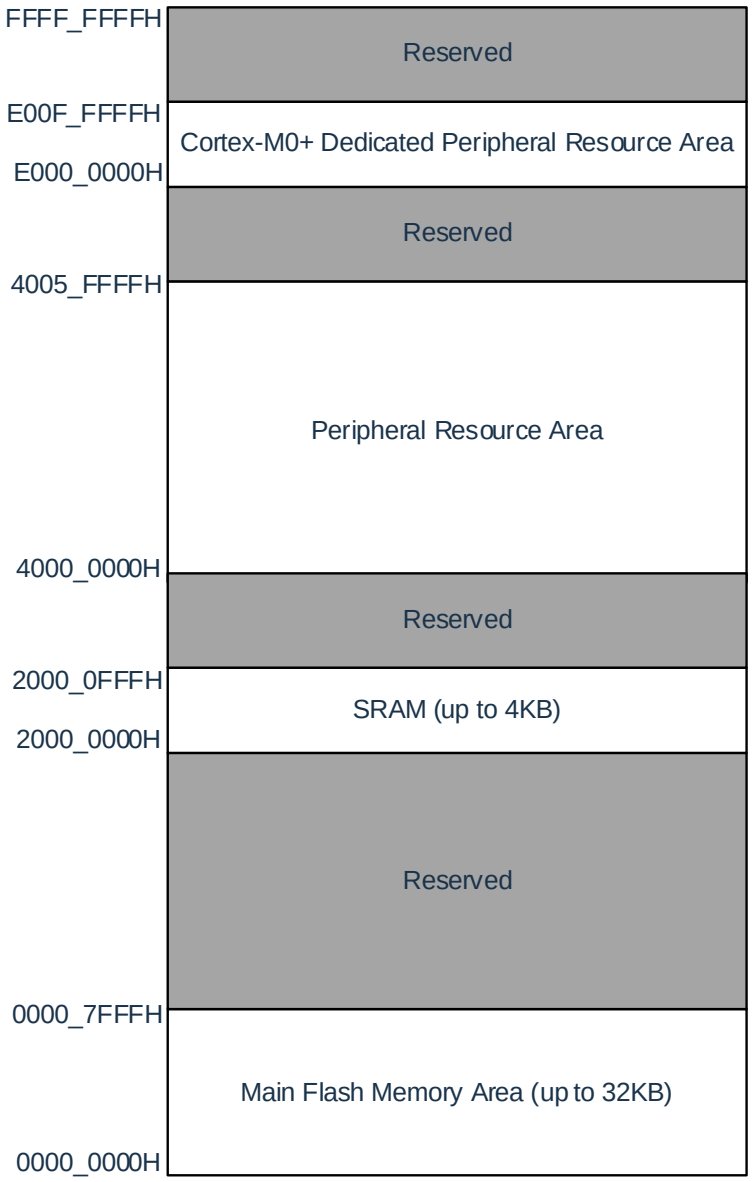
2 Product Structure Diagram



3 System Block Diagram



4 Memory Map


FFFF_FFFFH
Reserved
E00F_FFFFH
Cortex-M0+ Dedicated Peripheral Resource Area
E000_0000H
Reserved
4005_FFFFH
Peripheral Resource Area
4000_0000H
Reserved
2000_0FFFH
SRAM (up to 4KB)
2000_0000H
Reserved
0000_7FFFH
Main Flash Memory Area (up to 32KB)
0000_0000H

5 Pin Function

5.1 Port function

All ports of this product are categorized into 4 types, which are type 1, type 2, type 3 and type 4, and the corresponding situations are as follows:

Type 1: Bidirectional I/O function.

Type 2: Input function only, e.g. clock, corresponding to pins P121-P122.

Type 3: RESET function, corresponding to pin RESETB.

Type 4: Other functions, e.g. LIN, VSS/GND, Vcap

5.1.1 Pin description

Name	Type	I/O	After the reset is released	Multplexing function	Function
P00	Type 1	I/O	Analog function	ANI11/LTXD/VCIN10/TI00 /TBCLK0/(TAO0)/INTP8	Port 0 The 2-bit input/output ports can be designated as input or output in bit units. Input ports can be set by software using internal pull-up resistors. The inputs of P00 and P01 can be set as TTL input buffers, and the outputs can be set as N-channel open drain outputs (Vcap withstand voltage). P00 and P01 can be set as analog inputs.
P01				ANI10/LRXD/VCIN11/TO0 0/TBCLK1/TAIO0/INTP10/ (PGA1IN)	
P10		I/O	Analog function	ANI9/SPICLK/TMIOB1/(TMIOD1) /(TXD2/IrTxD)	Port 1 The 8-bit input/output ports can be designated as inputs or outputs in bit units. Inputs can be programmed by software using internal pull-up resistors. The inputs of P10, P14~P17 can be set as TTL input buffer. The outputs of P10, P11, P13~P15 and P17 can be set as N-channel open drain outputs (Vcap withstand voltage). P10 and P11 can be set as analog inputs.
P11				ANI8/MISO/(RxD0/SDI00)/TMIOD 1 /(TMIOA1/TMIOC1/TMIOB1)	
P12				SIMO/(TxD0/SDO00)/TMIOA1 /(TMIOB0/TMIOB1/TMIOC1)	
P13				TXD2/IrTxD/SDO20/TMIOC1 /(TMIOC0/TMIOD1/TMIOA1)	
P14				RXD2/IrRxd/SDI20/SDA20/TMI OB0 /(TMIOC1/TMIOD0)/(SCLA0)	
P15				SCLK20/SCL20/TMIOD0/(TMI OB0)/(SDAA0)/CLKBUZ1	
P16				TI01/TO01/INTP5/TMIOC0/(TMI OA1) /(RXD0)	
P17				TI02/TO02/TMIOA0/TMCLK0 /(TMIOD0)/(TXD0)	
P20		I/O	Analog function	ANI0/AVREFP/VCIN12/INTP11 /PGA0OUT	Port 2 The 4-bit input/output port can be designated as input or output in bit units. Can be set as analog input.
P21				ANI1/AVREFM/VCIN13	
P22				ANI2/ANO0/PGA0IN/VCIN0	
P23				ANI3/ANO1/PGA0GND	
P30		I/O	Input port	INTP3/SCLK00/SCL00/T AO0	Port 3

Name	Type	I/O	After the reset is released	Multplexing function	Function
				/(TMIOB1)	The 2-bit input/output ports can be designated as input or output in bit units. Input ports can be set by software using internal pull-up resistors. The inputs of P30 and P31 can be set as TTL input buffers, and the outputs can be set as N-channel open drain outputs (Vcap withstand voltage).
P31				TI03/TO03/INTP4/CLKBUZ0 /(TAIO0)/VCOUT1/SS00/SCLA 0	
P40		I/O	Input port	SWDIO/(TXD0/SDO00)	Port4 The 1-bit input/output port, can be designated as input or output. The input port can be set by software using an internal pull-up resistor.
P50		I/O	Input port	INTP1/SDI00/RXD0/SDA00 /TBIO0/(TAO0)/(TMIOC1)	Port5 The 2-bit input/output ports can be designated as input or output in bit units. Input ports can be set by software using internal pull-up resistors. The input of P50 can be set to TTL input buffer. The outputs of P50 and P51 can be set as N-channel open drain outputs (Vcap withstand voltage).
P51				INTP2/SDO00/TXD0/TBIO1 /(TMIOD1)	
P70		I/O	Input port	INTP6/(VCOUT1)	Port7 The 4-bit input/output ports can be designated as input or output in bit units. Input ports can be set by software using internal pull-up resistors. The inputs of the P72 can be set as TTL input buffers and the outputs can be set as N-channel open drain outputs (Vcap withstand voltage). If the LIN function is used, the P72 cannot be used as any other IO function and should be left floating.
P72				INTP7/(LTXD)	
P120		I/O	Analog function	ANI14/VCOUT0	Port 12 Of the 1-digit input/output ports and the 2-digit input-only ports, only the P120 has an output function. Only the inputs of the P120 can be set as analog inputs by the software, using the internal pull-up resistors.
P121	Type 2	I	Input port	X1	
P122				X2/EXCLK	
P136	Type 1	I/O	Input port	INTP0	Port 13 The 2-bit input/output ports can be set by software using internal pull-up resistors.
P137				SWCLK/(RXD0/SDI00)	
P147		I/O	Analog function	ANI12/VREF0/NSS/(PGA1GND)	Port14 The 1-bit input/output port can be designated as either input or output. The input port can be set by software, using an internal pull-up resistor. The P147 can be set to analog input.
RESETB	Type 3	I	-	-	A dedicated pin for external reset input, which must be connected to Vcap either directly or through a resistor when the external reset is not used.
LIN	Type 4	I/O	LIN communication	-	LIN bus input/output ports
Vcap		Power	-	-	LDO Output - It can supply power to the internal MCU and external devices and requires an external 0.1uF + 10uF decoupling capacitor.
Vbat		Power	-	-	Battery supply voltage

Name	Type	I/O	After the reset is released	Multplexing function	Function
GND/VSS		Ground	-	-	Ground

Remark:

1. Set each pin to digital or analog (can be set in bits) via Port Mode Control Register x (PMCx).
2. For the description of the multiplexing function, refer to “4.2 Port Multiplexing Function”.
3. The functions in ( ) in the above table can be assigned by setting the peripheral I/O redirection register.

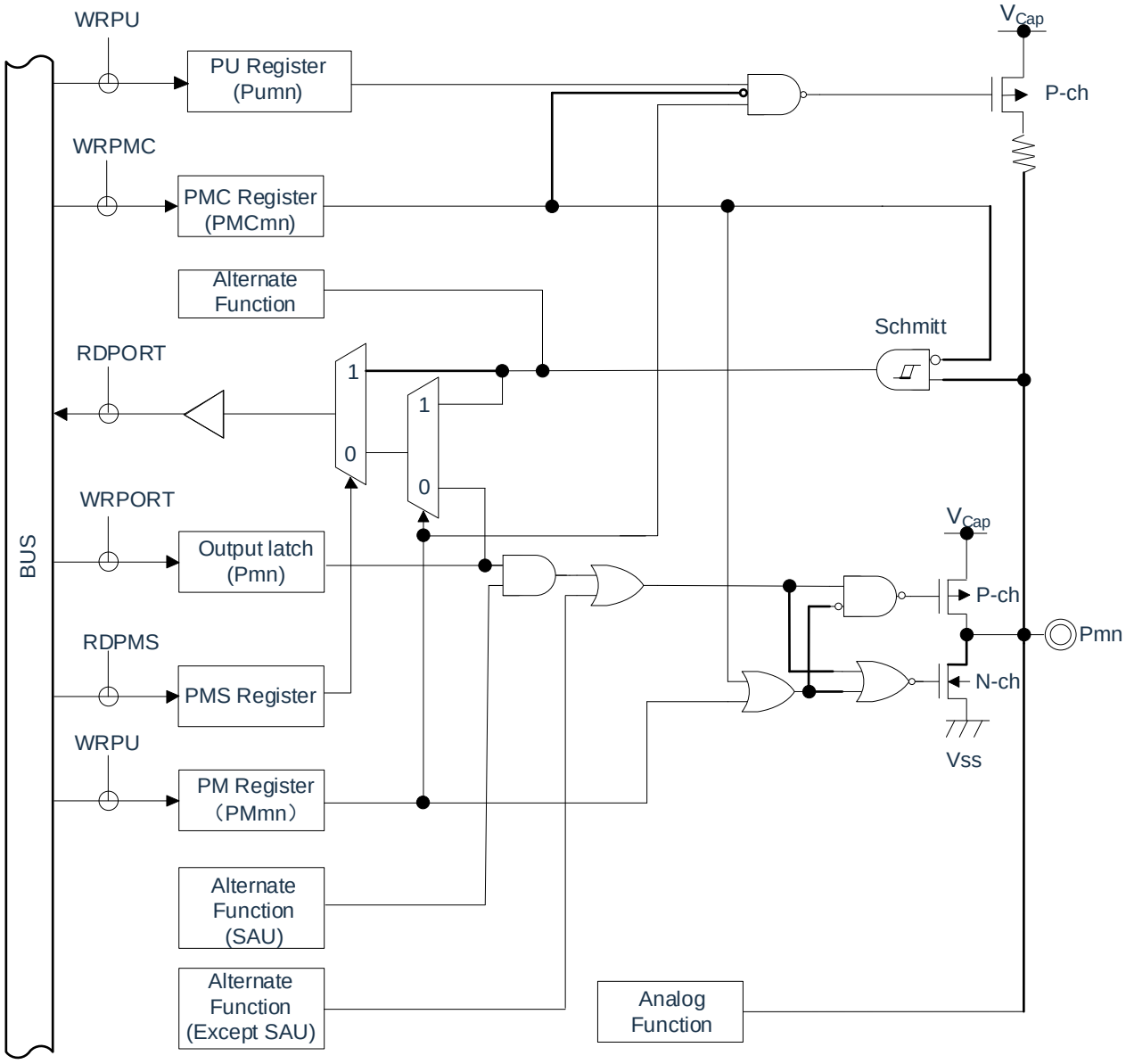
5.2 Port multiplexing function

Name	I/O	Function
ANI0~ANI3, ANI8~ANI12, ANI14	I	Analog input for A/D converters
ANO0, ANO1	O	D/A converter output
INTP0 ~ INTP8, INTP10~INTP11	I	External interrupt request input Designation of active edges: rising edge, falling edge, double edge
VCIN0	I	Analog voltage input for comparator 0
VCIN10~VCIN13	I	Analog voltage/reference input for comparator 1
VREF0	I	Reference voltage input for comparator 0
VCOUT0, VCOUT1	O	Comparator output
PGA0IN, PGA1IN	I	PGA input
PGA0GND, PGA1GND	I	PGA reference input
CLKBUZ0, CLKBUZ1	O	Clock output/buzzer output
RESETB	I	A system reset input that is active low and must be connected to Vcap either directly or through a resistor when an external reset is not used.
LRXD	I	Serial data input of LIN
LTXD	O	Serial data output of LIN
IrRxD	I	Serial data input of IrDA
IrTxD	O	Serial data output of IrDA
RxD0, RxD2	I	Serial data input of serial interfaces UART0, UART2
TxD0, TxD2	O	Serial data output of serial interfaces UART0,UART2
SCL00, SCL20	O	Serial clock output of serial interfaces IIC00, IIC20
SDA00, SDA20	I/O	Serial data input/output of serial interfaces IIC00, IIC20
SCLK00, SCLK20	I/O	Serial clock input/output of serial interfaces SSPI00, SSPI20
SDI00, SDI20	I	Serial data input of serial interfaces SSPI00, SSPI20
SS00	I	Chip select input of serial interface SSPI00
SDO00, SDO20	O	Serial data output of SSPI00, SSPI20
SCLA0	I/O	Serial clock input/output of serial interface IICA0
SDAA0	I/O	Serial data input/output of serial interface IICA0
SPICLK	I/O	Serial clock input/output of serial interface SPI
MISO	I/O	Serial data input/output of serial interface SPI
SIMO	I/O	Serial data input/output of serial interface SPI
NSS	I	Chip select input of serial interface SPI
TI00 ~TI03	I	External count clock/capture trigger input for 16-bit Timer4
TO00 ~TO03	O	Timer output for 16-bit Timer4
TAIO	I/O	TimerA inputs/outputs
TAO	O	TimerA outputs
TMCLK	I	External clock input for TimerM
TMIOA0, TMIOB0, TMIOC0, TMIOD0, TMIOA1, TMIOB1, TMIOC1, TMIOD1	I/O	TimerM inputs/outputs
TBIO0, TBIO1	I/O	TimerB inputs/outputs
TBCLK0, TBCLK1	I	External clock input for TimerB
X1, X2	—	Connect the resonator used for the main system clock
EXCLK	I	External clock input for main system clock
AV_{REFP}	I	Positive (+) reference voltage input for A/D converter

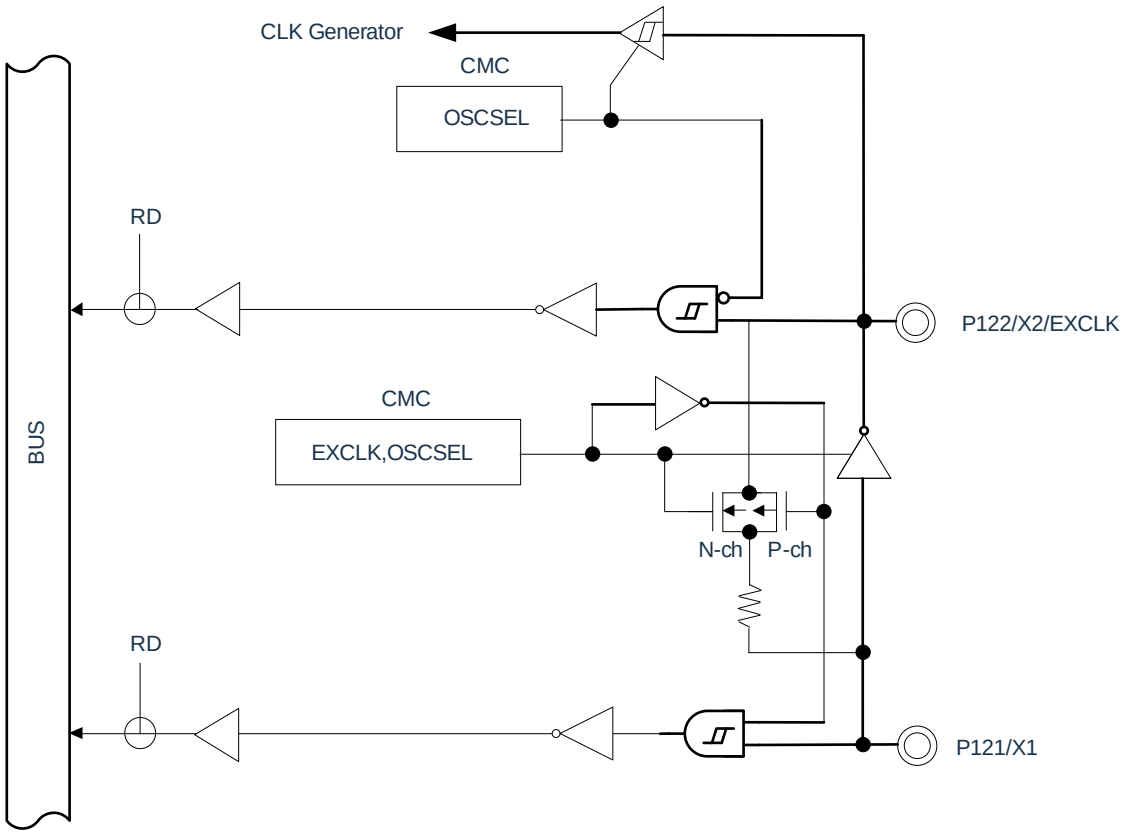
Name	I/O	Function
AV_{REFM}	I	Negative (-)A reference voltage input for A/D converter
SWDIO	I/O	SWD data interface
SWCLK	I	SWD clock interface
LIN	I/O	LIN bus input/output ports
V_{SS}	-	Power ground
GND	-	Power ground
Vbat	-	Battery supply voltage
Vcap	-	LDO Output - It can supply power to the internal MCU and external devices and requires an external 0.1uF + 10uF decoupling capacitor.

5.3 Port Type

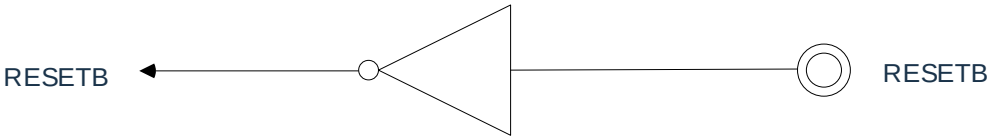
Type 1: Bidirectional I/ O capability



Type 2: Input function only



Type 3: RESET function



6 Functional Summary

6.1 ARM® Cortex®-M0+ core

ARM's Cortex-M0+ processor is the next generation of ARM processors for embedded systems. It provides a low-cost platform designed to meet the needs of low-pin-count and low-power microcontrollers while providing excellent computing performance and advanced system response to interrupts.

The Cortex-M0+ processor's 32-bit RISC processor provides superior code efficiency and delivers the high-performance expectations of an ARM core, unlike 8-bit and 16-bit devices of the same memory size. The Cortex-M0+ processor has 32 address lines and up to 4G of storage.

The BAT32A6300 uses an embedded ARM core, making it compatible with all ARM tools and software.

6.2 Memory

6.2.1 Flash memory

The BAT32A6300 has built-in flash memory that can be programmed, erased, and rewritten. It has the following functions:

- Programs and data share 32K storage.
- Support page erasure, the size of each page is 512byte.
- Support byte/ half-word/ word (32bit) programming.

6.2.2 SRAM

The BAT32A6300 contains 4KB of embedded SRAM.

6.3 Enhanced DMA controller

It has a built-in enhanced DMA (Direct Memory Access) controller that enables data transfer between memories without using the CPU.

- DMA can be started via peripheral function interrupts, enabling real-time control through communication, timers, and A/D.
- The transfer source/target field is optional for the full address space range (when the flash field is used as the target address, flash needs to be preset as the programming mode).
- Support 4 modes (normal transfer mode, repeat transfer mode, block transfer mode and chain transfer mode).

6.4 LIN transceiver

The BAT32A6300 is a local interconnect network (LIN) physical layer transceiver SoC with an integrated internal LDO. The internal LIN transceiver provides a stable 5V power supply for ECU (Electronic Control Unit) microcontrollers or related peripherals, and is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12V) and SAE J2602 standards. It is primarily suited for in-vehicle networks using transmission rates from 1kbps to 20kbps. The transceiver has an internal pull-up resistor on the LIN bus output pin and bus output waveform shaping to minimize electromagnetic emissions (EME). The transceiver is a full-duplex communicator, using the TXD pin as an input to transmit a low-voltage signal from the microcontroller to the LIN bus, while the LIN pin receives the data stream from the bus, and the receiver's output pin, RXD, transmits the data back to the microcontroller or to other microcontrollers.

The integrated internal LIN transceiver supports 12V applications over the 5.5V to 28V operating voltage range. The transceiver achieves very low current consumption in sleep mode, quickly minimizes power consumption in the event of a failure, and can be remotely woken up via the LIN bus or put into normal operating mode via a message on the EN pin. A power-up and power-down detection output pin, RSTN, is also provided for the 5V voltage regulator to monitor the power supply of the regulator.

6.5 Linkage controller

The linkage controller links the output events by each peripheral function with the peripheral function trigger sources. This enables collaborative operation between peripheral functions without using the CPU.

The linkage controller has the following functions:

- It can link event signals together to realize the linkage of peripheral functions.
- There are 20 types of event input and 9 types of event triggering.

6.6 Clock generation and startup

A clock generation circuit is a circuit that generates a clock to the CPU and peripheral hardware. There are three types of system clocks and clock oscillation circuits.

6.6.1 Main system clock

- X1 oscillation circuit: The resonator can be connected to pins (X1 and X2) to generate a clock oscillation of 1~20MHz, and the oscillation can be stopped by executing a deep sleep command or setting MSTOP.
- High-speed on-chip oscillator (high-speed OCO): Oscillation can be performed by selecting the frequency by the option byte. After released, the CPU starts running at this high-speed on-chip oscillator clock by default. Oscillation can be stopped by executing a deep sleep command or setting the HIOSTOP bit. The frequency set by the option byte can be changed through the frequency selection register of the high-speed on-chip oscillator. The maximum frequency is 64MHz with an accuracy ± 1.0%.
- Input external clock from pin (X2): (1~20MHz), and the input of the external main system clock can be invalidated by executing a deep sleep command or setting the MSTOP bit.

6.6.2 Low-speed on-chip oscillator clock

Low-speed on-chip oscillator (low-speed OCO): It generates a 15KHz (typical) clock oscillation. You cannot use a low-speed on-chip oscillator clock as a CPU clock. Only the following peripheral hardware can operate through the low-speed on-chip oscillator clock:

- Watchdog timer (WWDT).
- TimerA.

6.7 Power management

6.7.1 Power supply mode

Vbat: Battery supply voltage, voltage range 5.5V~28V, support 12V system.

Vcap: LDO output voltage 5V, voltage range 4.9V~5.1V, must be connected to 0.1uF and 10uF filter capacitor.

6.7.2 Power-on reset

The power-on reset circuit (POR) has the following functions.

- An internal reset signal is generated when power is applied. If the supply voltage (Vcap) is greater than the detection voltage (V_{POR}), the reset is released. However, the reset state must be maintained by a voltage detection circuit or an external reset until the operating voltage range is reached.
- Compare the supply voltage (Vcap) and the detection voltage (V_{POR}), when Vcap＜V_{POR} , an internal reset signal is generated. However, when the power supply drops, it must be shifted to the deep sleep mode or set to the reset state by the voltage detection circuit or external reset before falling below the operating voltage range. If operation is to be restarted, it must be verified that the power supply voltage has returned to within the operating voltage range.

6.7.3 Voltage detection

The voltage detection circuit sets the operating mode and detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) via option bytes. The voltage detection (LVD) circuit has the following functions:

- Compare the supply voltage (Vcap) and the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) and generate an internal reset or interrupt request signal.
- The sense voltage of the supply voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can be selected by the option byte.
- Can run in deep sleep mode.
- When the power supply rises, it must be maintained in the reset state by voltage detection circuitry or an external reset before reaching the operating voltage range. When the power supply drops, it must be switched to deep sleep mode before it is less than the operating voltage range, or set to reset by voltage detection circuit or external reset.
- The operating voltage range varies depending on the setting of the user option byte.

6.8 Low-power mode

The BAT32A6300 supports two low-power modes to achieve the best compromise between low power consumption, short start-up time, and available wake-up sources:

- Sleep mode: Sleep mode is entered by executing the sleep instruction. Sleep mode is a mode to stop the CPU running clock. If the high-speed system clock oscillator circuit or the high-speed on-chip oscillator is oscillating before the sleep mode is set, each clock continues to oscillate. Although this mode does not allow the operating current to be reduced to the level of deep sleep mode, it is an effective mode when processing is to be restarted immediately by an interrupt request or when frequent intermittent operation is to be performed.
- Deep sleep mode: Deep sleep mode is entered by executing the deep sleep instruction. Deep sleep mode is a mode that stops the oscillation of the high-speed system clock oscillator and high-speed on-chip oscillator and stops the whole system. The operating current of the chip can be greatly reduced. Since the deep sleep mode can be canceled by an interrupt request, intermittent operation is also possible. However, in the case of the X1 clock, since it is necessary to wait for the oscillation to stabilize when releasing the deep sleep mode, it is necessary to select the sleep mode if it is necessary to start processing immediately by an interrupt request.

In any of these modes, the registers, flags, and data memories remain as they were before being set to standby mode, and the status of the output latches and output buffers of the input/output ports is also maintained.

6.9 Reset function

The following seven methods generate a reset signal.

1) An external reset is input via the RESETB pin.
2) An internal reset is generated by program loop detection by the watchdog timer.
3) An internal reset is generated by comparing the supply voltage and the detection voltage of the power-on reset (POR) circuit.
4) An internal reset is generated by comparing the supply voltage and the detection voltage of the voltage detection circuit (LVD).
5) An internal reset occurs due to a RAM parity error.
6) An internal reset occurred due to access to illegal memory.
7) Software reset

The internal reset is the same as the external reset, and after the reset signal is generated, the procedure is executed from the addresses written in addresses 0000H and 0001H.

6.10 Interrupt function

The Cortex-M0+ processor has a built-in Nested Vector Interrupt Controller (NVIC) that supports up to 32 interrupt request (IRQ) inputs, one non-maskable interrupt (NMI) input, and multiple internal exceptions.

This product expands 32 maskable interrupt requests (IRQ) and 1 non-maskable interrupt (NMI) to support up to 64 maskable interrupt sources and one non-maskable interrupt source.

Maskable interrupt	External	5
	Internal	29

6.11 Watchdog timer

1-channel WWDT and 17-bit watchdog timer run via option byte set count. The watchdog timer operates on a low-speed on-chip oscillator clock (15KHz). Watchdog timers are used to detect program loops. When a program loop is detected, an internal reset signal is generated.

The following are judged to be program loop:

- When the watchdog timer counter overflows
- When a 1-bit operation instruction is executed on the watchdog timer enable register (WDTE).
- When writing data other than "ACH" to the WDTE register
- When writing data to the WDTE register during window closure

6.12 SysTick timer

This timer is exclusive to real-time operating systems, but can also be used as a standard decrement counter.

It is characterized by the generation of a maskable system interrupt when the 24-bit decrementing counter self-loading capacity counter reaches zero.

6.13 Timer4

This product has a built-in timer unit Timer4 containing four 16-bit timers. Each timer unit can be used as an independent timer or combined with multiple channels for advanced timer functions.

For details of each function, refer to the table below.

Independent channel operation function	Multi-channel linkage operation function
● Interval timer ● Square wave output ● External event counter ● Frequency divider ● Input pulse interval measurement ● Input signal high/low width measurement ● Delay counter	● Single trigger pulse output ● PWM output ● Multiple PWM outputs

6.13.1 Independent channel operation function

The independent channel operation function is a function that allows you to use any channel independently of other channel operation modes. The independent channel operation function is used in the following modes.

1) Interval timer: It can be used as a reference timer for generating interrupts at fixed intervals (INTTM).
2) Square wave output: Whenever an INTTM interrupt is generated, a flip is triggered to output a 50% duty cycle square wave from the timer output pin (TO).
3) External event counter: Count the effective edge of the input signal of the timer input pin (TI) and can be used as an event counter to generate an interrupt if the specified number of times is reached.
4) Divider function (limited to channel 0 of unit 0): divide the input clock of the timer input pin (TI00) and output it from the output pin (TO00).
5) Measurement of input pulse interval: The interval between input pulses is measured by starting counting at the effective edge of the input pulse signal at the timer input pin (TI) and capturing the count value at the effective edge of the next pulse.
6) High/low width measurement of input signal: Measure the high or low width of the input signal by starting counting on one edge of the input signal of the timer input pin (TI) and capturing the count value on the other edge.
7) Delay counter: Starts counting at the effective edge of the input signal at the timer input pin (TI) and generates an interrupt after an arbitrary delay period has elapsed.

6.13.2 Multi-channel linkage operation function

The multi-channel linkage operation function is a function that combines the master channel (the reference timer for the main control period) and the slave channel (the timer that follows the operation of the master channel). The multi-channel linkage function can be used in the following modes:

1) Single trigger pulse output: Two channels are used in pairs to generate a single trigger pulse that can arbitrarily set the output timing and pulse width.
2) PWM (Pulse Width Modulation) output: Two channels are used in pairs to generate pulses that can set the period and duty cycle arbitrarily.
3) Multiple PWM (Pulse Width Modulation) outputs: Up to 7 arbitrary duty-cycle PWM signals can be generated in fixed cycles by extending the PWM functionality and using 1 master channel and multiple slave channels.

6.13.3 8-bit timer operation function

The 8-bit timer operation function uses the 16-bit timer channel as the function of two 8-bit timer channels. (Only Channel 1 and Channel 3 can be used).

6.13.4 LIN-bus support function

The Timer4 unit can be used to check whether the received signal in the LIN-bus communication is suitable for the LIN-bus communication format.

1) Wake-up signal detection: The low-level width is measured by starting counting on the falling edge of the input signal on the UART serial data input pin (RxD) and capturing the count value on the rising edge. If the low width is greater than or equal to a fixed value, it is considered a wake-up signal.
2) Detection of the break field: After a wake-up signal is detected, the low-level width is measured by starting counting from the falling edge of the input signal of the UART serial data input pin (RxD) and capturing the count value on the rising edge. If the width of the low level is greater than or equal to a fixed value, it is considered to be a break field.
3) Measurement of sync field pulse width: After detecting the break field, measure the low- and high-level widths of the input signal of the UART serial data input pin (RxD). The baud rate is calculated from the bit interval of the synchronization field measured in this way.

6.14 TimerA

This product has a built-in 16-bit TimerA, consisting of a reload register and a decrement counter. Available for the following operating modes:

- Timer mode: Count the counting source (the counting source can be a clock or an external event)
- Pulse output mode: Count the counting source and output a pulse when overflowing
- Event counting mode: Count external events and works in deep sleep mode.
- Pulse width measurement mode: Measurement of external pulse width
- Pulse period measurement mode: Measurement of external pulse period

6.15 TimerM

This product has a built-in 2-channel 16-bit TimerM optimized for motor control, which has the following 4 operating modes:

- Timer mode:
  - Input capture function (external signal as trigger, count value to register)
  - Output comparison function (detect whether the count value and register value are the same, and can change the output of the pin during detection)
  - PWM function (continuous output of arbitrary pulse width)
- Reset synchronous PWM mode: output sawtooth wave modulation, three-phase waveforms without dead time (6 pcs)
- Complementary PWM mode: output triangle wave modulation, three-phase waveforms with dead time (6 pcs)
- PWM3 mode: output PWM waveforms with the same period (2 pcs)

6.16 TimerB

This product has a built-in 16-bit TimerB, which has the following 3 modes:

- Timer mode:
  - Input capture function counts on both sides of the rising edge, falling edge, or rising/ falling edge.
  - Output comparison function "L" level output, "H" level output or alternating output
- PWM mode: Can perform PWM output with arbitrary duty cycle.
- Phase counting mode: The counting value of the 2-phase encoder can be measured automatically.

6.17 TimerC

This product has a built-in 16-bit TimerC, which can be triggered by software, comparator or TimerM to realize the input capture function.

6.18 Clock output/buzzer output controller

The clock output controller is used to provide the clock to the peripheral IC, and the buzzer output controller is used to output the square wave of the buzzer frequency. The clock output or buzzer output is realized by dedicated pins.

6.19 Universal serial communication unit

This product has built-in 2 universal serial communication units, each unit has a maximum of 4 serial communication channels. It can implement standard SPI, simplified SPI, UART and simplified I^2C communication functions. Taking the 64-pin product as an example, the function distribution of each channel is as follows:

6.19.1 3-wire serial interface (simplified SPI)

Data is transmitted and received synchronously with the serial clock (SCK) output of the master device.

This is a clock-synchronous communication interface that communicates using a total of three communication lines: one serial clock (SCK), one transmit serial data (SO), and one receive serial data (SI).

[Data transmission and reception]

- Data length of 7 or 8 bits
- Phase control of data transmission and reception
- MSB/ LSB first

[Clock control]

- Master or slave selection
- Phase control of input/output clock
- Transfer cycles generated by prescalers and channel internal counters
- Maximum transfer rate

  Master communication: Max. $F_{CLK}/2$

  Slave communication: Max. $F_{MCK}/6$

[Interrupt function]

- Transfer end interrupt, buffer null interrupt

[Error detection flag].

- Overflow error

6.19.2 SPI with slave chip selection

The SPI serial communication interface supports slave chip select input function. This is a clock-synchronous communication interface that communicates using a slave chip select input (SSI), 1 serial clock (SCK), 1 transmit serial data (SO), and 1 receive serial data (SI) for a total of 4 communication lines.

[Data transmission and reception]

- Data length of 7 or 8 bits
- Phase control of transmitted and received data
- MSB/LSB first
- Level setting for transmitted and received data

[Clock control]

- Phase control of input/ output clocks
- Transfer cycles generated by prescalers and channel internal counters
- Maximum transfer rate

  Slave communication: Max. $F_{MCK}/6$

[Interrupt function]

- Transfer end interrupt, buffer null interrupt

[Error detection flag]

- Overflow error

6.19.3 UART

This function enables asynchronous communication over two lines, serial data transmission (TxD) and serial data reception (RxD). Using these two communication lines, data is transmitted and received asynchronously (using the internal baud rate) with other communicating parties in the data frame (consisting of start bits, data, parity bits, and stop bits). Full-duplex UART communication can be implemented by using two channels, dedicated to transmit (even channels) and dedicated to receiving (odd channels), and LIN-bus can also be supported by combining a Timer4 unit and an external interrupt (INTP0).

[Data transmission and reception]

- Data length of 7, 8, or 9 bits
- MSB/LSB first
- Level setting for transmitting and receiving data, selection of inversion
- Parity bit appending, parity check function
- Stop bit appending, stop bit detection

[Interrupt function]

- Transfer end interrupt, buffer null interrupt
- Error interrupts caused by frame errors, parity check errors, or overflow errors

[Error detection flag]

- Frame errors, parity errors, overflow errors

[LIN-bus function]

- Detection of wake-up signals
- Detection of break field (BF).
- Measurement of synchronous field, calculation of baud rate

6.19.4 Simplified I²C

This function enables clock synchronization communication with multiple devices via two lines, serial clock (SCL) and serial data (SDA). Because this simplified I²C is designed for single communication with devices such as flash memory and A/D converters, it can only be used as a master device. Start and stop conditions, like the operation control registers, must comply with the AC characteristics and are handled by software.

[Data transmission and reception]

- Master transmission, master reception (limited to the master function of single master)
- ACK output function, ACK detection function
- 8-bit data length (when transmitting the addresses, specify the addresses with the highest 7 bits, and use the lowest bit for R/W control).
- Start and stop conditions are generated by software

[Interrupt function]

- Transfer end interruption

[Error detection flag]

- ACK error, overflow error

[Simplified I²C unsupported features]

- Slave transmission, slave reception
- Multi-master function (arbitration failure detection function)
- Wait detection function

6.20 Standard serial interface IICA

The serial interface IICA has the following 3 modes:

1) Run-stop mode

   This is the mode used when serial transfer is not performed, which reduces power consumption.

2) I^2C bus mode (support multi-master)

   This mode transmits 8-bit data to multiple devices over 2 wires of a serial clock (SCLA) and a serial data bus (SDAA). In accordance with the I2C bus format, the master device can generate “start conditions”, “address”, “indication of transmission direction”, “data” and “stop conditions” on the serial data bus for the slave devices. The slave device automatically detects the received status and data by hardware. This feature simplifies the I^2C bus control part of the application program. Since the SCLA and SDAA pins of the serial interface IICA are used as open drain outputs, pull-up resistors are required for the serial clock line and the serial data bus.

3) Wake-up mode

   In deep sleep mode, when an extension code or a local station address is received from the master device, the deep sleep mode can be released by generating an interrupt request signal (INTIICA). This is set via the IICA control register.

6.21 LIN/UART module (LIN)

This product is equipped with a LIN communication controller that supports LIN protocols including 1.3, 2.0, 2.1, 2.2, and SAEJ 2602 standards, and features automatic inter-frame communication and error detection. The LIN/UART module provides a UART mode and can be used as a single UART.

The module has the following functions.

1) LIN communication function
   - ➢ It can be used as a master or a slave
   - ➢ It has a variable frame structure

     Master: 13~28Tbits interval transfer width; 1~4Tbits interval character transfer width; 0~7Tbits byte interval (frame header); 0~7Tbits response interval; 0~3Tbits interval between data bytes in response area; 1~16Tbits wake-up interval.

     Slave: 9.5 or 10.5Tbits (fixed baud rate) interval receive width, 10 or 11Tbits (auto baud rate); 0 to 7Tbits response interval; 0 to 3Tbits interval between data bytes in the response area; 1 to 16Tbits wake-up interval.
   - ➢ The response field data is between 0 and 8 bytes, and more than 9 bytes of response can be transmitted and received.
   - ➢ It provides LIN wake-up mode
   - ➢ Support multiple state detection
   - ➢ Support for generating multiple interrupts

     Successful header/frame/wakeup transfer/reception interrupt, successful frame/wakeup transfer/reception interrupt, error detection interrupt
   - ➢ Support for user-assessed self-testing models
2) UARTcommunication function

   [Data transmission and reception]
   - ➢ Data length of 7, 8 bits (support 9-bit, including extension bits)
   - ➢ MSB/LSB first
   - ➢ Level setting for transmitting and receiving data, selection of inversion
   - ➢ Parity bit appending, parity function
   - ➢ Stop bit appending, stop bit detection

   [Interrupt function]
   - ➢ Transfer start/success interrupt
   - ➢ Successful receive interrupt
   - ➢ Status detection interrupt

   [Status flag]
   - ➢ Support multiple status flag detection

6.22 Analog-to-digital converter (ADC)

This product has a built-in 12-bit resolution analog-to-digital converter (SARADC) that converts analog inputs to digital values and supports up to 13 channels of ADC analog inputs (ANI0~ANI3, ANI8~ANI12, ANI14). The ADC contains the following functions:

- 12-bit resolution, slew rate: 1.06Msps.
- Triggering mode: support software triggering, hardware triggering and hardware triggering in standby state.
- Channel selection: support single-channel select mode and multi-channel scan mode.
- Conversion mode: support single conversion and continuous conversion.
- Operating voltage: support 2.0V≤Vcap≤5.5V operating voltage range.
- It can detect the built-in reference voltage (1.45V/2.4V) and temperature sensors.
- The reference voltage source can be selected from: 1.45V/2.4V/Vcap

The ADC can set various A/D conversion modes by combining the modes described below.

Trigger mode	Software trigger	Start the conversion by operating the software.
	Hardware-trigger no-wait mode	The conversion is started by detecting a hardware trigger.
	Hardware trigger wait mode	In the conversion standby state when the power is cut off, the power is turned on by detecting the hardware trigger, and the conversion starts automatically after the A/D power stabilization waiting time.
Channel select mode	Select mode	Select 1 channel of analog input for A/D conversion.
	Scan mode	Convert the analog inputs of 4 channels sequentially to A/D. 4 consecutive channels from ANI0 to ANI3, ANI8 to ANI12, and ANI14 can be selected as analog inputs.
Conversion mode	Single conversion mode	Perform an A/D conversion for the selected channel.
	Continuous conversion mode	Perform continuous A/D conversions for the selected channel until stopped by the software.
Sample time/ conversion time	Number of sample clocks/ conversion clocks	The sampling time can be set by register, the default value of sampling clock number is 13.5 clk, and the minimum value of conversion clock number is 31.5 clk.

6.23 Digital-to-analog converter (DAC)

This product has a built-in 2-channel 12-bit resolution analog-to-digital converter (DAC) that converts digital inputs to analog signals. It has the following features:

- 12-bit resolution D/A converter
- Support two independent analog channel outputs
- The reference voltage source can be selected from: 1.45V/2.4V/Vcap
- R-2R ladder network
- Built-in real-time output
- Reset-hold function

6.24 Programmable gain amplifier (PGA)

This product has a built-in programmable gain amplifier (PGA0) with the following functions:

- There are 8 choices of amplification gain per PGA: 1x, 2.5x, 4x, 8x, 10x, 16x, 32x.
- External pin as ground for the PGA negative feedback resistor (can be used as differential mode) is selectable
- The output of PGA0 can be selected as an analog input for the A/D converter or an analog input on the positive side of comparator 0 (CMP0)
- Reference voltage can be selected from 1/2Vcap or internal reference voltage (1.45V/2.4V)
- PGA output = input x gain + reference voltage

6.25 Comparator (CMP)

This product has a built-in two-channel comparator, CMP0 and CMP1, with the following functions:

- The negative side of the CMP can be selected as an external pin input, internal reference voltage or DAC output voltage.
- The positive side of CMP0 can be selected as an external pin input or PGA0 output; the positive side of CMP1 can be selected as external pin inputs (4 pcs)
- Able to select the cancellation width of noise-canceling digital filters
- Able to detect the active edge of the comparator output and generate an interrupt signal.
- Able to detect the active edge of the comparator output and output the event signal to the linkage controller.
- In combination with other functions, the initial motor position can be detected and high/low speed rotation can be controlled.
- Combined with Timer4, TIMER WINDOW can be output.
- Support positive hysteresis, negative hysteresis, and bilateral hysteresis for comparators with selectable hysteresis voltages of 20mV, 40mV, and 60mV.
- Support 12-bit DAC as negative input source

6.26 Two-wire serial debug port (SW-DP)

The ARM's SW-DP interface allows connection to the microcontroller via a serial line debugging tool.

6.27 Safety function

6.27.1 Flash CRC function (High-speed CRC, universal CRC)

Data errors in flash memory are detected by CRC operations.

The following two CRCs can be used for different applications and conditions of use.

- High-speed CRC: In the initialization program, it can stop the CPU and check the whole code flash area at high speed.
- Universal CRC: Can be used for multi-purpose checking during CPU operation, not limited to the code flash area.

6.27.2 RAM parity error detection function

Detect parity error when reading RAM data.

6.27.3 SFR protection function

Prevent rewriting of important SFRs (Special Function Registers) due to loss of CPU control.

6.27.4 Illegal memory access detection function

Detect illegal access to an illegal memory area (an area with no memory or an area with restricted access).

6.27.5 Frequency detection function

Able to use the Timer4 unit to self-test the CPU or peripheral hardware clock frequency.

6.27.6 A/D test function

The A/D converter is self-tested by A/D converting the positive (+) reference voltage, the negative (-) reference voltage, the analog input channel (ANI), the temperature sensor output voltage, and the internal reference voltage.

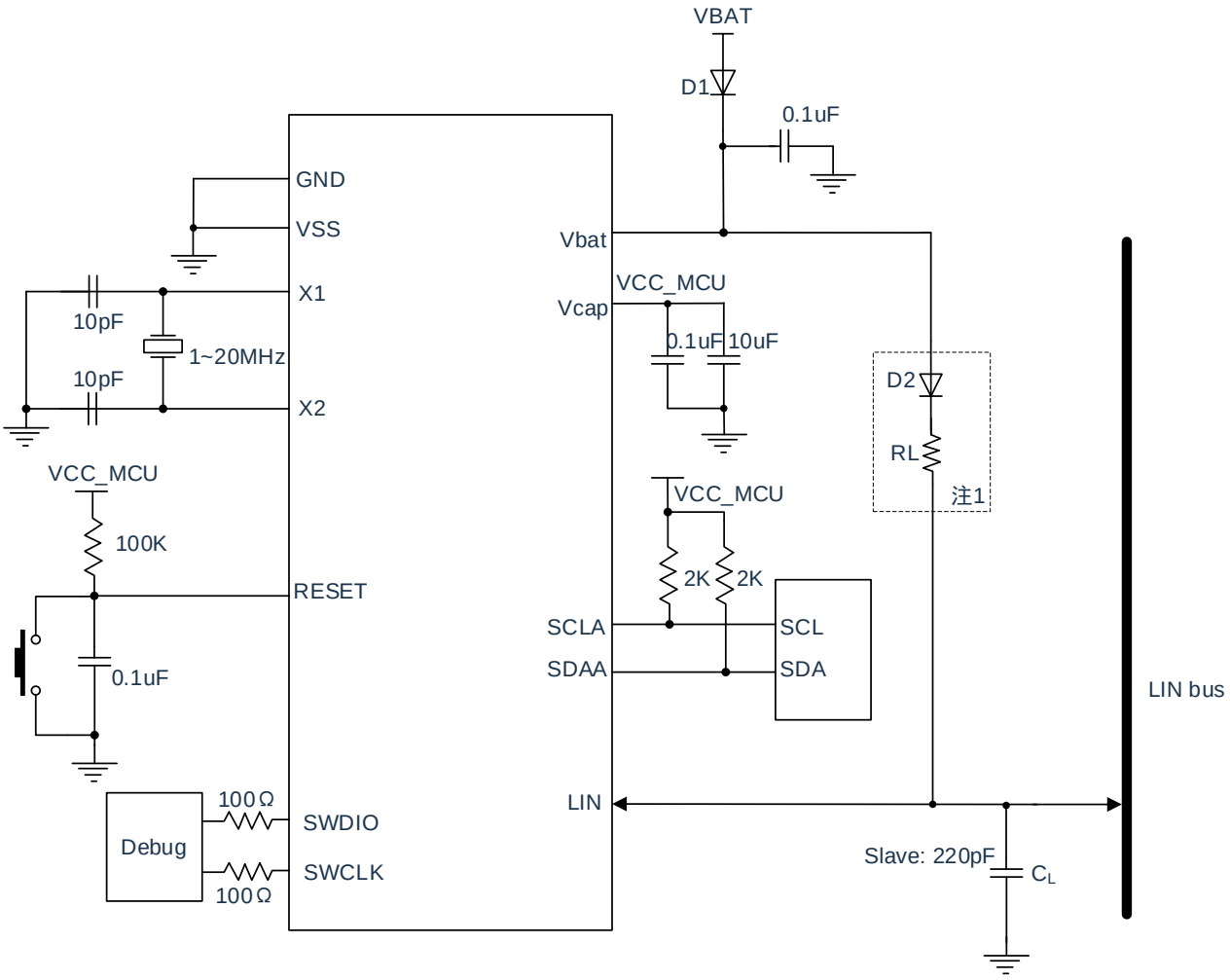
6.27.7 Digital output signal level detection function for input/output ports

When the input/output port is in output mode, the output level of the pin can be read.

7 Electrical Characteristics

7.1 Typical application peripheral circuits

The reference diagram for the connection of peripheral circuits for typical MCU applications is as follows:



Note 1: Connect D2, RL only when used as a master node.

Note 2: For master node, it is recommended to use 660Ω/6.8nF RL/CL to obtain a slower slope of the bus waveform.

7.2 Absolute maximum voltage rating

(T_A= -40~125°C)

Item	Symbol	Condition	Rating	Unit
Battery voltage	Vbat	-	-0.3~40	V
MCU voltage	Vcap	-	-0.5~6.5	V
Input voltage	V_{I1}	P00~P01, P10~P17, P30, P40 P50~P51, P70, P72, P120, P136, P147	-0.3~Vcap+0.3[Note1]	V
	V_{I2}	P20~P23, P121~P122, P137, EXCLK RESETB	-0.3~Vcap+0.3[Note1]	V
Output voltage	V_{O1}	P00~P01, P10~P17, P30, P40 P50~P51, P70~P72, P120, P136, P147	-0.3~Vcap+0.3[Note1]	V
	V_{O2}	P20~P23, P137	-0.3~Vcap+0.3[Note1]	V
Analog input voltage	V_{AI1}	ANI8~ANI12, ANI14	-0.3~Vcap+0.3 and -0.3~AV_{REF} (+)+0.3[Note1,2]	V
	V_{AI2}	ANI0~ ANI3	-0.3~Vcap+0.3 and -0.3~AV_{REF} (+)+0.3[Note1,2]	V

Note 1: No more than 6.5V.

Note 2: The pins of the A/D conversion object must not exceed AV_{REF} (+)+0.3.

Notice: Even if one item in each item instantly exceeds the absolute maximum rating, it may reduce the quality of the product. The absolute maximum rating is the rating that may cause physical damage to the product, and the product must be used in a state that does not exceed the rated value.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. AV_{REF} (+): The positive (+) reference voltage of the A/D converter
3. Use V_{SS} as the reference voltage.
4. This specification is guaranteed by the design, and is not tested in mass production.

7.3 Absolute maximum current rating

(T_A= -40~125℃)

Item	Symbol	Condition		Rating	Unit
Output current, high	I_{OH1}	Per pin	P00~P01, P10~P17, P30, P40 P50~P51, P70, P72, P120, P136~P137, P147	-40	mA
		Total -170mA	P00~P01, P40, P120, P136~P137	-70	mA
			P10~P17, P30~P31, P50~P51, P70, P72 P147	-100	mA
	I_{OH2}	Per pin	P20~P23	-3	mA
		Total		-15	mA
Output current, low	I_{OL1}	Per pin	P00~P01, P10~P17, P30, P40 P50~P51, P70, P72, P120 P136~P137, P147	40	mA
		Total 170mA	P00~P01, P40, P120, P136~P137	100	mA
			P10~P17, P30, P50~P51, P70, P72, P147	120	mA
	I_{OL2}	Per pin	P00~P01, P10~P17, P30, P40, P50~P51 P70, P72, P120, P136~P137, P147	15	mA
		Total		45	mA
Input negative current	I_{INJL}	Each pin	Continuous DC negative current that can be injected into an input pin	-3	mA
		Pin total		-15	mA
Input positive current	I_{INJH}	Each pin	Continuous DC positive current that can be injected into an input pin	3	mA
		Pin total		15	mA
Operating ambient temperature	T_A	Usually runtime		-40~125	℃
		When programming the flash memory			
Storage temperature	T_{stg}	-		-65~150	℃

Notice: Even if one item in each item instantly exceeds the absolute maximum rating, it may reduce the quality of the product. The absolute maximum rating is the rating that may cause physical damage to the product, and the product must be used in a state that does not exceed the rated value.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. This specification is guaranteed by the design, and is not tested in mass production

7.4 Oscillation circuit characteristics

7.4.1 X1, XT1 characteristics

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=0V)

Item	Resonator	Condition	Min.	Typ.	Max.	Unit
X1 clock oscillation frequency (F_X)	Ceramic/crystal resonator	-	1.0	-	20.0	MHz
X1 clock oscillation stabilization time	Ceramic/crystal resonator	20MHz, C=10pF	-	15	-	ms
X1 clock oscillation feedback resistor	Ceramic/crystal resonator	-	0.6	-	1.8	MΩ

Remark:

1. It only indicates the frequency tolerance range of the oscillation circuit, and the instruction execution time should be referred to the AC characteristics.
2. Please ask the resonator manufacturer to evaluate the circuit after installation, and use it after confirming the oscillation characteristics.

7.4.2 Internal oscillator characteristics

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=0V)

Resonator	Condition	Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency (F_{IH})Note1,2	-	1.0	-	64.0	MHz
High-speed on-chip oscillator stabilization time (T_{SU})	-	-	12	-	us
Clock frequency accuracy of high-speed on-chip oscillator	T_A= 10~70℃	-1.0	-	+1.0	%
	T_A= 0~105℃	-1.5	-	+1.5	%
	T_A= -10~125℃	-2.0	-	+2.0	%
	T_A= -40~125℃	-3.0	-	+3.0	%
Low-speed on-chip oscillator clock frequency (F_{IL})	-	10	15	22	KHz

Note 1: Select the frequency of the high-speed on-chip oscillator via the option byte.

Note 2: It only indicates the characteristics of the oscillation circuit, so please refer to the AC characteristics for the instruction execution time.

7.5 DC characteristics

7.5.1 Pin characteristics

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output current, high[Note1]	I_{OH1}	P00~P01, P10~P17 P30~P31, P40, P50~P51 P70, P72~P74, P120 136, P147 Per pin	2.0V≤Vcap≤5.5V -40~85℃	-	-	-12.0[Note2]	mA
			2.0V≤Vcap≤5.5V 85~125℃	-	-	-6.0[Note2]	
		P00~P01, P40, P120 P136 Total (when duty cycle≤70%[Note3])	4.0V≤Vcap≤5.5V -40~85℃	-	-	-60.0	mA
			4.0V≤Vcap≤5.5V 85~125℃	-	-	-30.0	
			2.4V≤Vcap<4.0V	-	-	-12.0	mA
			2.0V≤Vcap<2.4V	-	-	-6.0	mA
		P10~P17, P30~P31 P50~P51, P70, P72~P74 P147 Total (when duty cycle≤70%[Note3])	4.0V≤Vcap≤5.5V -40~85℃	-	-	-80.0	mA
			4.0V≤Vcap≤5.5V 85~125℃	-	-	-30.0	
			2.4V≤Vcap<4.0V	-	-	-20.0	mA
			2.0V≤Vcap<2.4V	-	-	-10.0	mA
		Total (when duty cycle≤70%[Note3])	4.0V≤Vcap≤5.5V -40~85℃	-	-	-140.0	mA
			4.0V≤Vcap≤5.5V 85~125℃	-	-	-60.0	
			2.4V≤Vcap<4.0V	-	-	-30.0	
			2.0V≤Vcap<2.4V	-	-	-15.0	
	I_{OH2}	P20~P23,P137 per pin	2.0V≤Vcap≤5.5V	-	-	-2.5[Note2]	mA
		Total (when duty cycle≤70% [Note3])	2.0V≤Vcap≤5.5V	-	-	-10	mA

Note 1: This is the value of current that guarantees device operation even if current flows from the Vcap pin to the output pin.

Note 2: The total current value cannot be exceeded.

Note 3: This is the output current value for the “Duty cycle ≤ 70% condition”. The following formula can be used to calculate the output current value when the duty cycle is changed to >70% (when the duty cycle is changed to n%).

Total pin output current=(I_{OH}×0.7)/(n×0.01)

<Calculation example>I_{OH}= -10.0mA, n=80%

Total pin output current= (-10.0×0.7)/(80×0.01) ≈ -8.7mA

The current at each pin does not vary by duty cycle and will not flow above the absolute maximum rating.

Notice: In N-channel open drain mode, P00~P01, P10~P11, P13~P15, P17, P30~P31, P50~P51, P72, P74 do not output high level.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output current, low[Note1]	I_{OL1}	P00~P01, P10~P17 P30~P31, P40 P50~P51, P70 P72~P74, P120 P136, P147 Per pin	2.0V≤Vcap≤5.5V -40~85℃	-	-	30[Note2]	mA
			2.0V≤Vcap≤5.5V 85~125℃	-	-	15[Note2]	mA
		P00~P01, P40, P120 P136 Total (when duty cycle ≤70%[Note3])	4.0V≤Vcap≤5.5V -40~85℃	-	-	100	mA
			4.0V≤Vcap≤5.5V 85~125℃	-	-	50	mA
			2.4V≤Vcap＜4.0V	-	-	30	mA
			2.0V≤Vcap＜2.4V	-	-	15	mA
		P10~P17, P30~P31 P50~P51, P70 P72~P74, P147 Total (when duty cycle ≤70%[Note3])	4.0V≤Vcap≤5.5V -40~85℃	-	-	120	mA
			4.0V≤Vcap≤5.5V 85~125℃	-	-	60	mA
			2.4V≤Vcap＜4.0V	-	-	40	mA
			2.0V≤Vcap＜2.4V	-	-	20	mA
		Total (when duty cycle ≤70%[Note3])	4.0V≤Vcap≤5.5V -40~85℃	-	-	150	mA
			4.0V≤Vcap≤5.5V 85~125℃	-	-	80	mA
			2.4V≤Vcap＜4.0V	-	-	50	mA
			2.0V≤Vcap＜2.4V	-	-	30	mA
	I_{OL2}	P20~P23,P137 per pin	2.0V≤Vcap≤5.5V	-	-	6[Note2]	mA
		Total (when duty cycle ≤70%[Note3])	2.0V≤Vcap≤5.5V	-	-	20	mA

Note 1: This is the value of current at which the V_{SS} pin guarantees device operation even if current flows from the output pin to the EV_{SS}.

Note 2: The total current value cannot be exceeded.

Note 3: This is the output current value for the “Duty cycle ≤ 70% condition”. The following formula can be used to calculate the output current value when the duty cycle is changed to >70% (n% duty cycle).

Total output current=(I_{OL}×0.7)/(n×0.01)

<Calculation example>I_{OL}=10.0mA, n=80%

Total output current=(10.0×0.7)/(80×0.01) ≈ 8.7mA

The current at each pin does not vary by duty cycle and will not flow above the absolute maximum rating.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Battery voltage	Vbat	-		5.5		28	V
MCU input voltage	Vcap	-		4.9	-	5.1	V
Power ground input voltage	V_{SS}	-		-0.3	-	-	V
Input voltage, high	V_{IH1}	P00~P01, P10~P17 P30~P31, P40 P50~P51, P70 P72~P74, P120 P136, P147	Schmidt input	0.8Vcap	-	Vcap	V
	V_{IH2}	P00~P01, P10 P14~P17, P30~P31 P50, P72, P74	TTL input 4.0V≤Vcap≤5.5V	2.2	-	Vcap	V
			TTL input 3.3V≤Vcap＜4.0V	2.0	-	Vcap	V
			TTL input 2.0V≤Vcap＜3.3V	1.5	-	Vcap	V
	V_{IH3}	P20~P23, P137		0.7Vcap	-	Vcap	V
	V_{IH4}	P121~P122, EXCLK, RESETB		0.8Vcap	-	Vcap	V
Input voltage, low	V_{IL1}	P00~P01, P10~P17 P30~P31, P40 P50~P51, P70 P72~P74, P120 P136, P147	Schmidt input	0	-	0.2Vcap	V
	V_{IL2}	P00~P01, P10 P14~P17, P30~P31 P50, P72, P74	TTL input 4.0V≤Vcap≤5.5V	0	-	0.8	V
			TTL input 3.3V≤Vcap＜4.0V	0	-	0.5	V
			TTL input 2.0V≤Vcap＜3.3V	0	-	0.32	V
	V_{IL3}	P20~P23, P137		0	-	0.3Vcap	V
	V_{IL4}	P121~P122, EXCLK, RESETB		0	-	0.2Vcap	V

Notice: Even in N-channel open drain mode, the maximum VIH value for P00~P01, P10~P11, P13~P15, P17, P30~P31, P50~P51, P72, P74 is Vcap.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40 ~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output voltage, high	V_{OH1}	P00~P01, P10~P17 P30~P31, P40 P50~P51, P70 P72~P74, P120 P136, P147	4.0V≤Vcap≤5.5V I_{OH1}= -12.0mA	Vcap-1.5	-	-	V
			4.0V≤Vcap≤5.5V I_{OH1}= -6.0mA	Vcap-0.7	-	-	V
			2.4V≤Vcap≤5.5V I_{OH1}= -3.0mA	Vcap-0.6	-	-	V
			2.0V≤Vcap≤5.5V I_{OH1}= -2mA	Vcap-0.5	-	-	V
	V_{OH2}	P20~P23,P137	4.0V≤Vcap≤5.5V I_{OH2}= -2.5mA	Vcap-1.5	-	-	V
			4.0V≤Vcap≤5.5V I_{OH2}= -1.5mA	Vcap-0.7	-	-	V
			2.4V≤Vcap≤5.5V I_{OH2}= -0.5mA	Vcap-0.6	-	-	V
			2.0V≤Vcap≤5.5V I_{OH2}= -0.4mA	Vcap-0.5	-	-	V
Output voltage, low	V_{OL1}	P00~P01, P10~P17 P30~P31, P40 P50~P51, P70 P72~P74, P120 P136, P147	4.0V≤Vcap≤5.5V I_{OL1}=30.0mA	-	-	1.2	V
			4.0V≤Vcap≤5.5V I_{OL1}=15.0mA	-	-	0.7	V
			2.4V≤Vcap≤5.5V I_{OL1}=6.0mA	-	-	0.4	V
			2.0V≤Vcap≤5.5V I_{OL1}=4.0mA	-	-	0.4	V
	V_{OL2}	P20~P23,P137	4.0V≤Vcap≤5.5V I_{OL2}=6.0mA	-	-	1.2	V
			4.0V≤Vcap≤5.5V I_{OL2}=4.0mA	-	-	0.7	V
			2.4V≤Vcap≤5.5V I_{OL2}=1.5mA	-	-	0.4	V
			2.0V≤Vcap≤5.5V I_{OL2}=1.0mA	-	-	0.4	V

Notice: In N-channel open drain mode, P00~P01, P10~P11, P13~P15, P17, P30~P31, P50~P51, P72, P74 do not output high level.

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Input leakage current, high	I_{LIH1}	P00~P01, P10~P17 P30~P31, P40 P50~P51, P70 P72~P74, P120 P136, P147	V_I= Vcap	-	-	1	uA
	I_{LIH2}	P20~P23, P137 RESETB	V_I=Vcap	-	-	2	uA
	I_{LIH3}	P121~P122 (X1, X2 EXCLK)	V_I=Vcap, when the input port and external clock are inputting	-	-	1	uA
			V_I=Vcap, when connecting the resonator	-	-	10	uA
Input leakage current, low	I_{LIL1}	P00~P01, P10~P17 P30~P31, P40 P50~P51, P70 P72~P74, P120 P136, P147	V_I=V_{SS}	-	-	-1	uA
	I_{LIL2}	P20~P23, P137 RESETB	V_I=V_{SS}	-	-	-2	uA
	I_{LIL3}	P121~P121 (X1, X2 EXCLK)	V_I=V_{SS}, when the input port and external clock are inputting	-	-	-1	uA
			V_I=V_{SS}, when connecting the resonator	-	-	-10	uA
Internal pull-up resistance	R_U	P00~P01, P10~P17 P30~P31, P40 P50~P51, P70 P72~P74, P120 P136~P137, P147	V_I=V_{SS}, When inputting a port	10	30	100	KΩ

Remark:

1. Unless otherwise specified, the characteristics of the multiplexing pin are the same as the characteristics of the port pin.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

7.5.2 Power supply current characteristics

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition				Min.	Typ.	Max.	Unit
Supply current[Note1]	I_{DD1}	Run mode	High-speed on-chip oscillator	F_{HOCO}=64MHz, F_{IH}=64MHz[Note3]		-	5.0	13.5	mA
				F_{HOCO}=48MHz, F_{IH}=48MHz[Note3]		-	4.5	11.0	
				F_{HOCO}=32MHz, F_{IH}=32MHz[Note3]		-	4.0	8.5	
			High-speed master system clock	F_{MX}=20MHz[Note2]	Input square wave	-	3.5	7.0	mA
					Connect the crystal oscillator	-	3.5	7.0	
			Low-speed on-chip oscillator	F_{IL}=15KHz[Note4]			65	140	uA
	I_{DD2}	Sleep mode	High-speed on-chip oscillator	F_{HOCO}=64MHz, F_{IH} =64MHz[Note3]		-	1.8	10.0	mA
				F_{HOCO}=48MHz, F_{IH} =48MHz[Note3]		-	1.6	7.5	
				F_{HOCO}=32MHz, F_{IH} =32MHz[Note3]		-	1.2	5.0	
			High-speed master system clock	F_{MX} =20MHz[Note2]	Input square wave	-	1.0	4.5	mA
					Connect the crystal oscillator	-	1.0	4.5	
			Low-speed on-chip oscillator	F_{IL}=15KHz[Note4]		-	6	35	uA
	I_{DD3}	Deep sleep mode[Note6]	T_A= -40℃~25℃ Vcap=5.0V			-	1.5	3	uA
			T_A= -40℃~85℃ Vcap=5.0V			-	1.5	10	
			T_A= -40℃~105℃ Vcap=5.0V			-	1.5	15	
			T_A= -40℃~125℃ Vcap=5.0V			-	1.5	50	

Note 1: This is the current that flows through Vcap, including the input leakage current when the input pin is fixed to Vcap or V_{SS}, EV_{SS} state. Typical value: CPU is in multiplication instruction execution (IDD1), and does not include peripheral operating current. Maximum value: CPU is executing multiplication instruction (I_{DD1}), and includes peripheral operating current, but does not include current flowing to A/D converter, LVD circuit, I/O ports, internal pull-up or pull-down resistors, and does not include current when rewriting data flash memory.

Note 2: This is the case when the high-speed on-chip oscillator and low-speed on-chip oscillator clocks stop oscillating.

Note 3: This is the case when the high-speed main system clock and the low-speed on-chip oscillator clock stop oscillating.

Note 4: This is the case when the high-speed on-chip oscillator and the high-speed main system clock stop oscillating.

Note 5: This is the case when the high-speed on-chip oscillator and the high-speed main system clock stop oscillating.

Note 6: For current values when the low-speed on-chip oscillator clock is running in deep sleep mode, refer to Current values when the low-speed on-chip oscillator clock is running in sleep mode.

Remark:

1. F_{HOCO}: High-speed on-chip oscillator clock frequency, F_{IH}: The system clock frequency provided by the high-speed on-chip oscillator.
2. F_{MX}: External master system clock frequency (X1/X2 clock oscillation frequency).
3. The temperature condition of the typical value is TA = 25°C.

（T_A= -40~125℃、Vbat = 12V、V_{SS}=GND=0V）

Item	Symbol	Condition				Min.	Typ.	Max.	Unit
Vbat pin current	I_{bat1}	Run mode note1	High-speed on-chip oscillator	F_{HOCO}=64MHz、F_{IH}=64MHz		-	7.5	17.5	mA
				F_{HOCO}=48MHz、F_{IH}=48MHz		-	7	15	
				F_{HOCO}=32MHz、F_{IH}=32MHz		-	6.5	12.5	
			High-speed master system clock	F_{MX}=20MHz	Input square wave	-	6	11	mA
					Connect the crystal oscillator	-	6	11	
			Low-speed on-chip oscillator	F_{IL}=15KHz			2.56	4.1	mA
	I_{bat2}	Sleep mode note2	High-speed on-chip oscillator	F_{HOCO}=64MHz、F_{IH} =64MHz		-	1.9	10.2	mA
				F_{HOCO}=48MHz、F_{IH} =48MHz		-	1.7	7.7	
				F_{HOCO}=32MHz、F_{IH} =32MHz		-	1.3	5.2	
			High-speed master system clock	F_{MX} =20MHz	Input square wave	-	1.1	4.7	mA
					Connect the crystal oscillator	-	1.1	4.7	
			Low-speed on-chip oscillator	F_{IL}=15KHz		-	48	79	uA
	I_{bat3}	Deep sleep mode Note3	T_A= -40℃~25℃			-	42	48	uA
			T_A= -40℃~85℃			-	55	67	
			T_A= -40℃~105℃			-	68	89	
			T_A= -40℃~125℃			-	85	110	
	I_{bat4}	Stop mode note4	T_A= -40℃~125℃			-	10	55	uA

Note 1: Run mode, this refers to the MCU is in the running state, the LIN transceiver is working normally, the LDO outputs 5V and the maximum drive current is 70mA.

Note 2: Sleep mode, this refers to stopping the CPU running clock, the peripherals can work according to the setting, the LIN transceiver is in standby, the LDO continuously outputs 5V with a 70 mA driving capacity, and the system can be woken up by an external interrupt.

Note 3: Deep sleep mode, this refers to the high-speed system clock and the whole system stops, the LIN transceiver is in standby state, the LDO continuously outputs 5V with a drive current of 70 mA, and the system can be woken up by an external interrupt.

Note 4: Stop mode, this means the LDO stops outputting 5V, the MCU is in power-down state, the LIN transceiver is in sleep state, and the system can be woken up remotely via the LIN bus.

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Low speed on-chip oscillator operating current	I_{FIL} Note1,8	-		-	0.2	-	uA
WDT operating current	I_{WDT} Note1,2,3,8	F_{IL}=15KHz		-	0.22	-	uA
A/D converter operating current	I_{ADC} Note1,4	ADC HS mode@64MHz		-	2.2	-	mA
		ADC HS mode@4MHz		-	1.3	-	mA
		ADC LC mode@24MHz		-	1.1	-	mA
		ADC LC mode@4MHz		-	0.8	-	mA
D/A converter operating current	I_{DAC} Note1,6	Per channel		-	1.4	-	mA
PGA operating current		Per channel		-	900	1400	uA
Comparator operating current	I_{CMP} Note1,7	Per channel	No internal reference voltage is used	-	60	100	uA
			An internal reference voltage is used	-	80	160	uA
LVD operating current	I_{LVD} Note1,5,8	-		-	0.08	-	uA

Note 1: This is the current flowing through Vcap.

Note 2: This is when the high-speed on-chip oscillator and the high-speed system clock stop oscillating.

Note 3: This is the current that flows only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). With the watchdog timer running, the microcontroller current value is the value of I_{DD1} or I_{DD2} or I_{DD3} plus IWDT.

Note 4: This is the current that flows only to the A/D converter. With the A/D converter running in run mode or sleep mode, the microcontroller current value is I_{DD1} or I_{DD2} plus the value of I_{ADC}.

Note 5: This is the current that flows only to the LVD circuit. With the LVD circuit running, the microcontroller current value is the value of I_{DD1} or I_{DD2} or I_{DD3} plus I_{LVD}.

Note 6: This is the current that flows only to the D/A converter. With the D/A converter running in run mode or sleep mode, the microcontroller current value is the value of I_{DD1} or I_{DD2} plus I_{DAC}.

Note 7: This is the current that flows only to the comparator circuit. With the comparator circuit running, the microcontroller current value is the value of I_{DD1} or I_{DD2} or I_{DD3} plus I_{CMP}.

Note 8: Low temperature specification is guaranteed by the design, and is not tested in mass production.

Remark:

1. F_{IL}: Low-speed on-chip oscillator clock frequency
2. The temperature condition of the typical value is T_A=25℃.

7.6 AC characteristics

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (F_{MAIN}) is running	2.0V≤Vcap≤5.5V	0.02084	-	1	us
External system clock frequency	F_{EX}	2.0V≤Vcap≤5.5V		1.0	-	20.0	MHz
	F_{EXS}	2.0V≤Vcap≤5.5V		32.0	-	35.0	KHz
High and low level width of external system clock input	T_{EXH}, T_{EXL}	2.0V≤Vcap≤5.5V		24	-	-	ns
	T_{EXHS}, T_{EXLS}	2.0V≤Vcap≤5.5V		13.7	-	-	us
TI00 ~ TI03, input high- and low-level widths	T_{TIH}, T_{TIL}	2.0V≤Vcap≤5.5V		$1/F_{MCK}$+10	-	-	ns
Input period of TimerA	T_C	TAIO	2.4V≤Vcap≤5.5V	100	-	-	ns
			2.0V≤Vcap＜2.4V	300	-	-	ns
High- and low-level widths of TimerA input	T_{TAIH}, T_{TAIL}	TAIO	2.4V≤Vcap≤5.5V	40	-	-	ns
			2.0V≤Vcap＜2.4V	120	-	-	ns

Remark:

1. F_{MCK}: Operation clock frequency of the Timer4 unit.
2. Low temperature specification is guaranteed by the design, and is not tested in mass production.

(T_A= -40~125°C, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Timer M input high- and low-level widths	T_{TMIH}, T_{TMIL}	TMIOA0, TMIOA1, TMIOB0, TMIOB1, TMIOC0, TMIOC1, TMIOD0, TMIOD1		3/F_{CLK}	-	-	ns
Timer M Forced cutoff signal input low level width	T_{TMSIL}	P136/INTP0	2MHz＜F_{CLK}≤48MHz	1	-	-	us
			F_{CLK} ≤2MHz	1/F_{CLK} +1	-	-	us
High- and low-level width of TimerB input	T_{TBIH}, T_{TBIL}	TBIOA, TBIOB		2.5/F_{CLK}	-	-	ns
TO00 ~ TO03, TAIO0, TAO0, TMIOA0, TMIOA1, TMIOB0, TMIOB1, TMIOC0, TMIOC1, TMIOD0, TMIOD1, TBIOA, TBIOB output frequency	F_{TO}	4.0V≤Vcap≤5.5V		-	-	16	MHz
		2.4V≤Vcap＜4.0V		-	-	8	MHz
		2.0V≤Vcap＜2.4V		-	-	4	MHz
CLKBUZ0, CLKBUZ1 output frequency	F_{PCL}	4.0V≤Vcap≤5.5V		-	-	16	MHz
		2.4V≤Vcap＜4.0V		-	-	8	MHz
		2.0V≤Vcap＜2.4V		-	-	4	MHz
High- and low-level width of interrupt input	T_{INTH}, T_{INTL}	INTP0~INTP11	2.0V≤Vcap≤5.5V	1	-	-	us
RESETB low-level width	T_{RSL}	-		10	-	-	us

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

7.7 Peripheral function characteristics

7.7.1 Universal interface unit

(1) UART mode

(T_A= -40~85℃, 2.0V≤Vcap≤5.5V, VSS=GND=0V)

Item	Condition		Specification value		Unit
			Min.	Max.	
Transfer rate	2.0V ≤Vcap ≤ 5.5V	-	-	F_{MCK} /6	bps
		Theoretical value of the maximum transfer rate F_{MCK} = F_{CLK}	-	8	Mbps

(T_A=+85~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Condition		Specification value		Unit
			Min.	Max.	
Transfer rate	2.0V ≤Vcap ≤ 5.5V	-	-	F_{MCK} /12	bps
		Theoretical value of the maximum transfer rate F_{MCK} = F_{CLK}	-	4	Mbps

Remark: This specification is guaranteed by the design, and is not tested in mass production.

(2) 3-wire SPI mode (master mode, internal clock output)

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		-40~85℃		85~125℃		Unit
				Min.	Max.	Min.	Max.	
SCLKp cycle time	T_{KCY1}	T_{KCY1}≥2/F_{CLK}	4.0V ≤Vcap ≤ 5.5V	41.67	-	83.33	-	ns
			2.7V ≤Vcap ≤ 5.5V	83.33	-	166.67	-	ns
			2.4V ≤Vcap ≤ 5.5V	125	-	250	-	ns
			2.0V ≤Vcap ≤ 5.5V	250	-	500	-	ns
SCLKp high/low level width	T_{KH1}, T_{KL1}	4.0V ≤Vcap ≤ 5.5V		T_{KCY1}/2-7	-	T_{KCY1}/2-14	-	ns
		2.7V ≤Vcap ≤ 5.5V		T_{KCY1}/2-10	-	T_{KCY1}/2-20	-	ns
		2.4V ≤Vcap ≤ 5.5V		T_{KCY1}/2-18	-	T_{KCY1}/2-36	-	ns
		2.0V ≤Vcap ≤ 5.5V		T_{KCY1}/2-38	-	T_{KCY1}/2-76	-	ns
SDIp set-up time (for SCLKp↑)	T_{SIK1}	4.0V ≤Vcap ≤ 5.5V		23	-	46	-	ns
		2.7V ≤Vcap ≤ 5.5V		33	-	66	-	ns
		2.4V ≤Vcap ≤ 5.5V		44	-	88	-	ns
		2.0V ≤Vcap ≤ 5.5V		75	-	113	-	ns
SDIp hold time (for SCLKp↑)	T_{KSI1}	2.0V ≤Vcap ≤ 5.5V		10	-	20	-	ns
Delay time from SCLKp↓→SDOp	T_{KSO1}	2.0V ≤Vcap ≤ 5.5V C=20pF[Note1]		-	10	-	20	ns

Note 1: C is the load capacitance of the SCLKp, SDOp output lines.

Notice: Through the Port Input Mode Register and Port Output Mode Register, the SDIp pin is selected as the normal input buffer and the SDOp pin and SCLKp pin are selected as the normal output mode.

Remark: This specification is guaranteed by the design, and is not tested in mass production.

(3) 3-wire SPI mode (slave mode, external clock input)

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition		-40~85℃		85~125℃		Unit
				Min.	Max.	Min.	Max.	
SCLKp cycle time	T_{KCY2}	4.0V ≤Vcap ≤ 5.5V	20MHz＜ F_{MCK}	8/F_{MCK}	-	16/F_{MCK}	-	ns
			F_{MCK} ≤20MHz	6/F_{MCK}	-	12/F_{MCK}	-	ns
		2.7V ≤Vcap ≤ 5.5V	16MHz ＜ F_{MCK}	8/F_{MCK}	-	16/F_{MCK}	-	ns
			F_{MCK} ≤16MHz	6/F_{MCK}	-	12/F_{MCK}	-	ns
		2.4V ≤Vcap ≤ 5.5V		6/F_{MCK} and ≥500	-	12/F_{MCK} and ≥1000	-	ns
		2.0V ≤Vcap ≤ 5.5V		6/F_{MCK} and ≥750	-	12/F_{MCK} and ≥1500	-	ns
SCLKp high/low level width	T_{KH2} T_{KL2}	4.0V ≤Vcap ≤ 5.5V		T_{KCY1}/2-7	-	T_{KCY1}/2-14	-	ns
		2.7V ≤Vcap ≤ 5.5V		T_{KCY1}/2-8	-	T_{KCY1}/2-16	-	ns
		2.0V ≤Vcap ≤ 5.5V		T_{KCY1}/2-18	-	T_{KCY1}/2-36	-	ns
SDIp set-up time (for SCLKp↑)	T_{SIK2}	2.7V ≤Vcap ≤ 5.5V		1/F_{MCK}+20	-	1/F_{MCK} +40	-	ns
		2.0V ≤Vcap ≤ 5.5V		1/F_{MCK}+30	-	1/F_{MCK} +60	-	ns
SDIp hold time (for SCLKp↑)	T_{KSI2}	2.0V ≤Vcap ≤ 5.5V		1/F_{MCK}+31	-	1/F_{MCK} +62	-	ns
Delay time from SCLKp↓ →SDOp	T_{KSO2}	2.7V ≤Vcap ≤ 5.5V C=30pF[Note1]		-	2/F_{MCK}+44	-	2/F_{MCK}+66	ns
		2.4V ≤Vcap ≤ 5.5V C=30pF[Note1]		-	2/F_{MCK}+75	-	2/F_{MCK}+113	ns
		2.0V ≤Vcap ≤ 5.5V C=30pF[Note1]		-	2/F_{MCK}+100	-	2/F_{MCK}+150	ns

Note 1: C is the load capacitance of the SCLKp, SDOp output lines.

Notice: Through the Port Input Mode Register and Port Output Mode Register, the SDIp and SCLKp pins are selected as the normal input buffers and the SDOp pin is selected as the normal output mode.

Remark: This specification is guaranteed by the design, and is not tested in mass production.

(4) 4-wire SPI mode (slave mode, external clock input)

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, VSS=GND=0V)

Item	Symbol	Condition		-40~85℃		85~125℃		Unit
				Min.	Max.	Min.	Max.	
SSI00 set-up time	T_{SSIK}	DAPmn=0	2.7V ≤Vcap ≤ 5.5V	120	-	240	-	ns
			2.0V ≤Vcap ≤ 5.5V	200	-	400	-	ns
		DAPmn=1	2.7V ≤Vcap ≤ 5.5V	$1/F_{MCK}$+120	-	$1/F_{MCK}$+240	-	ns
			2.0V ≤Vcap ≤ 5.5V	$1/F_{MCK}$+200	-	$1/F_{MCK}$+400	-	ns
SSI00 hold time	T_{KSSI}	DAPmn=0	2.7V ≤Vcap ≤ 5.5V	$1/F_{MCK}$+120	-	$1/F_{MCK}$+240	-	ns
			2.0V ≤Vcap ≤ 5.5V	$1/F_{MCK}$+200	-	$1/F_{MCK}$+400	-	ns
		DAPmn=1	2.7V ≤Vcap ≤ 5.5V	120	-	240	-	ns
			2.0V ≤Vcap ≤ 5.5V	200	-	400	-	ns

Notice: Select the SDIp and SCLKp pins as the normal input buffers and the SDOp pin as the normal output mode via the Port Input Mode Register and Port Output Mode Register.

Remark: This specification is guaranteed by the design, and is not tested in mass production.

(5) Simplified IIC mode

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, VSS=GND=0V)

Item	Symbol	Condition	-40~85℃		85~125℃		Unit
			Min.	Max.	Min.	Max.	
SCLr clock frequency	F_{SCL}	2.7V ≤Vcap ≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	-	1000Note 1	-	400Note 1	KHz
		2.0V ≤Vcap ≤ 5.5V C_b = 100 pF, R_b = 3KΩ	-	400Note1	-	100Note 1	KHz
		2.0V ≤Vcap ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	-	300Note1	-	75Note1	KHz
Hold time when SCLr is low	T_{LOW}	2.7V ≤Vcap ≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	475	-	1200	-	ns
		2.0V ≤Vcap ≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	1150	-	4600	-	ns
		2.0V ≤Vcap ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	1550	-	6500	-	ns
Hold time when SCLr is high	T_{HIGH}	2.7V ≤Vcap ≤ 5.5V C_b = 50 pF, R_b = 2.7KΩ	475	-	1200	-	ns
		2.0V ≤Vcap ≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	1150	-	4600	-	ns
		2.0V ≤Vcap ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	1550	-	6500	-	ns
Data setup time (reception)	$T_{SU:DAT}$	2.7V ≤Vcap ≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	$1/F_{MCK}$+85Note2	-	$1/F_{MCK}$+220Note2	-	ns
		2.0V ≤Vcap ≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	$1/F_{MCK}$+145Note 2	-	$1/F_{MCK}$+580Note2	-	ns
		2.0V ≤Vcap ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	$1/F_{MCK}$+230Note 2	-	$1/F_{MCK}$+1200Note 2	-	ns
Data hold time (transmission)	$T_{HD:DAT}$	2.7V ≤Vcap ≤ 5.5V C_b = 50 pF, R_b = 2.7KΩ	-	305	-	770	ns
		2.0V ≤Vcap ≤ 5.5V C_b = 100 pF, R_b = 3KΩ	-	355	-	1420	ns
		2.0V ≤Vcap ≤ 2.7V C_b = 100 pF, R_b = 5KΩ	-	405	-	2070	ns

Note 1: The value must also be equal to or less than F_{MCK}/4.

Note 2: Set the F_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Remark: This specification is guaranteed by the design, and is not tested in mass production.

7.7.2 Serial interface IICA

1) I²C standard mode

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLA0 clock frequency	F_{SCL}	Standard mode: F_{CLK}≥1MHz	-	100	KHz
Set-up time of the start condition	$T_{SU: STA}$	-	4.7	-	us
Hold time of the start condition Note1	$T_{HD: STA}$	-	4.0	-	us
Hold time when SCLA0 is low	T_{LOW}	-	4.7	-	us
Hold time when SCLA0 is high	T_{HIGH}	-	4.0	-	us
Data set-up time (reception)	$T_{SU: DAT}$	-	250	-	ns
Data hold time (transmission) Note2	$T_{HD: DAT}$	-	0	3.45	us
Set-up time of the stop condition	$T_{SU: STO}$	-	4.0	-	us
Bus idle time	T_{BUF}	-	4.7	-	us

Note 1: Generate the first clock pulse after a start condition or a restart condition is generated.

Note 2: The maximum value of $T_{HD: DAT}$ needs to be guaranteed during normal transfer and needs to be waited during acknowledger (ACK).

Notice: The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (pull-up resistor value of the communication line) at this time are as follows:

Standard mode: C_b=400pF, R_b=2.7KΩ

Remark: This specification is guaranteed by the design, and is not tested in mass production.

2) I²C fast mode

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLA0 clock frequency	F_{SCL}	Fast mode: F_{CLK}≥3.5MHz		400	KHz
Set-up time of the start condition	$T_{SU: STA}$	-	0.6	-	us
Hold time of the start condition Note1	$T_{HD: STA}$	-	0.6	-	us
Hold time when SCLA0 is low	T_{LOW}	-	1.3	-	us
Hold time when SCLA0 is high	T_{HIGH}	-	0.6	-	us
Data set-up time (reception)	$T_{SU: DAT}$	-	100	-	ns
Data hold time (transmission) Note2	$T_{HD: DAT}$	-	0	0.9	us
Set-up time of the stop condition	$T_{SU: STO}$	-	0.6	-	us
Bus idle time	T_{BUF}	-	1.3	-	us

Note 1: Generate the first clock pulse after a start condition or a restart condition is generated.

Note 2: The maximum (MAX.) value of $T_{HD: DAT}$ needs to be guaranteed during normal transfer and needs to be waited during acknowledger (ACK).

Notice: The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (pull-up resistor value of the communication line) at this time are as follows:

Fast mode: C_b=320pF, R_b=1.1KΩ

Remark: This specification is guaranteed by the design, and is not tested in mass production.

3) I^2C enhanced fast mode

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLA0 clock frequency	F_{SCL}	Enhanced fast mode: F_{CLK}≥10MHz	-	1000	KHz
Set-up time of the start condition	$T_{SU: STA}$	-	0.26	-	us
Hold time of the start condition Note1	$T_{HD: STA}$	-	0.26	-	us
Hold time when SCLA0 is low	T_{LOW}	-	0.5	-	us
Hold time when SCLA0 is high	T_{HIGH}	-	0.26	-	us
Data set-up time (reception)	$T_{SU: DAT}$	-	50	-	ns
Data hold time (transmission) Note2	$T_{HD: DAT}$	-	0	0.45	us
Set-up time of the stop condition	$T_{SU: STO}$	-	0.26	-	us
Bus idle time	T_{BUF}	-	0.5	-	us

Note 1: Generate the first clock pulse after a start condition or restart condition is generated.

Note 2: The maximum value of $T_{HD: DAT}$ needs to be guaranteed during normal transfer and needs to be waited during acknowledger (ACK).

Notice: The maximum value of C_b (communication line capacitance) for each mode and the value of R_b (pull-up resistor value of the communication line) at this time are as follows:

Enhanced fast mode: C_b=120pF, R_b=1.1KΩ

Remark: This specification is guaranteed by the design, and is not tested in mass production.

7.8 Analog characteristics

7.8.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel \ Reference voltage	Reference voltage (+)=AV_{REFP} Reference voltage (-)=AV_{REFM}	Reference voltage (+)=Vcap Reference voltage (-)=V_{SS}
ANI0~ANI3, ANI8~ANI12, ANI14	Refer to 7.8.1 (1)	Refer to 7.8.1 (2)
Internal reference voltage, temperature sensor output voltage		

(1) When selecting reference voltage(+)=AV_{REFP}/ANI0, reference voltage(-)=AV_{REFM}/ANI1
(T_A= -40~125℃, 2.0V≤AV_{REFP}≤Vcap=Vcap≤5.5V, V_{SS}=0V, reference voltage(+)=AV_{REFP}, reference voltage(-)= AV_{REFM} =0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Resolution	RES	-		-	12	-	bit
Overall error[Note1]	ET	12-bit resolution	2.0V ≤ AV_{REFP}≤ 5.5V	-	3	-	LSB
Zero-scale error[Note1]	E_{ZS}	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-	0	-	LSB
Full-scale error[Note1]	E_{FS}	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-	0	-	LSB
Integral linearity error[Note1]	EL	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-1	-	1	LSB
Differential linearity error[Note1]	ED	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-1.5	-	1.5	LSB
Conversion time[Note3]	T_{CONV}	12-bit resolution Conversion target: ANI0~ANI3, ANI8~ANI12, ANI14	2.0V ≤Vcap≤ 5.5V	45	-	-	1/F_{ADC}
		12-bit resolution Conversion target: internal reference voltage, temperature sensor output voltage, PGA output voltage.	2.0V ≤Vcap≤ 5.5V	72	-	-	1/F_{ADC}
External input resistance	R_{AIN}	R_{AIN} ＜ (Ts / (F_{ADC} x C_{ADC} x ln (2^{12+2}))- R_{ADC})		-	10[Note4]	-	KΩ
Sampling switch resistance	R_{ADC}	-		-	-	1.5	KΩ
Sample-and-hold capacitance	C_{ADC}	-		-	2	-	pF
Analog input voltage	V_{AIN}	ANI0~ANI3, ANI8~ANI12, ANI14		0	-	AV_{REF}	V
		Internal reference voltage (2.0V≤Vcap≤5.5V)		V_{BGR}[Note2]			V
		Temperature sensor output voltage (2.0V≤Vcap≤5.5V)		V_{TMPS25}[Note2]			V

Note 1: Excludes quantization error (±1/2 LSB).

Note 2: Refer to “7.8.2 Characteristics of temperature sensor/internal reference voltage”.

Note 3: F_{ADC} is the operation frequency of the AD, and the maximum operation frequency is 48MHz.

Note 4: This specification is guaranteed by the design, and is not tested in mass production. Its typical value is the default sampling period, Ts=13.5, and the conversion speed is calculated under the condition of F_{ADC}=48MHz.

(2) When selecting reference voltage(+)=Vcap, reference voltage (-)=V_{SS}

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V, reference voltage (+)=Vcap, reference voltage (-)=V_{SS})

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Resolution	RES	-		-	12	-	bit
Overall error[Note1]	ET	12-bit resolution	2.0V ≤AV_{REFP}≤5.5V	-	6	-	LSB
Zero-scale error[Note1]	E_{ZS}	12-bit resolution	2.0V ≤AV_{REFP}≤5.5V	-	0	-	LSB
Full-scale error[Note1]	E_{FS}	12-bit resolution	2.0V ≤AV_{REFP}≤5.5V	-	0	-	LSB
Integral linearity error[Note1]	EL	12-bit resolution	2.0V ≤AV_{REFP}≤5.5V	-2	-	2	LSB
Differential linearity error[Note1]	ED	12-bit resolution	2.0V ≤AV_{REFP}≤5.5V	-3	-	3	LSB
Conversion time[Note3]	T_{CONV}	12-bit resolution Conversion target: ANI0~ ANI3, ANI8~ANI12, ANI14	2.0V≤Vcap≤5.5V	45	-	-	1/F_{ADC}
		12-bit resolution Conversion target: Internal reference voltage, temperature sensor output voltage, PGA output voltage.	2.0V≤Vcap≤5.5V	72	-	-	1/F_{ADC}
External input resistance	R_{AIN}	R_{AIN} ＜ (T_S / (F_{ADC} x C_{ADC} x ln (2^{12+2}))- R_{ADC})		-	10^{Note4}	-	KΩ
Sampling switch resistance	R_{ADC}	-		-	-	1.5	KΩ
Sample-and-hold capacitance	C_{ADC}	-		-	2	-	pF
Analog input voltage	V_{AIN}	ANI0~ANI3, ANI8~ANI12, ANI14		0	-	Vcap	V
		Internal reference voltage (2.0V≤Vcap≤5.5V)		V_{BGR}[Note2]			V
		Temperature sensor output voltage (2.0V≤Vcap≤5.5V)		V_{TMPS25}[Note2]			V

Note 1: Excludes quantization error (±1/2 LSB).

Note 2: Refer to “7.8.2 Characteristics of temperature sensor/internal reference voltage”.

Note 3: F_{ADC} is the operation frequency of the AD, and the maximum operation frequency is 48MHz.

Note 4: This specification is guaranteed by the design, and is not tested in mass production. Its typical value is the default sampling period, T_S=13.5, and the conversion speed is calculated under the condition of F_{ADC}=48MHz.

7.8.2 Characteristics of temperature sensor/internal reference voltage

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Temperature sensor output voltage	V_{TMPS25}	T_A=25℃	-	1.09	-	V
Internal reference voltage	V_{BGR}	T_A= -40~10℃	1.30	1.45	1.60	V
		T_A=10~70℃	1.38	1.45	1.52	V
		T_A=70~125℃	1.35	1.45	1.55	V
		T_A= -40~10℃	2.15	2.40	2.65	V
		T_A=10~70℃	2.28	2.40	2.52	V
		T_A=70~125℃	2.23	2.40	2.57	V
Temperature coefficient	F_{VTMPS}	-	-	-3.2	-	mV/℃
Operation stabilization wait time	T_{AMP}	-	5	-	-	us

Remark: This specification is guaranteed by the design, and is not tested in mass production

7.8.3 D/A converter

(Unless otherwise specified , T_A=25℃, V_{DD}=5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
operating current	I_{VDD}	Input code =800, T_A= -40~125℃		0.4	1	1.5	mA
Turn-off current	I_{SD}	T_A= -40~125℃		-	0.01	5	uA
Resolution	RES	-	-	-	-	12	bit
Overall error	ET	Buffer off	-	-	±6	-	LSB
		Buffer on			±8	-	
Differential nonlinear error	DNL				±4	-	LSB
Offset voltage	Vosbuf	Buffer offset voltage			±5	-	mV
Output range	Vout	Buffer off		1		V_{REF}-1	LSB
		Buffer on	Refer to V_{DD}	0.3		V_{DD}-0.3	V
			Refer to V_{REF}, V_{DD}≥3V	0.3		V_{REF}	V
Output load	R_{LAOD}			5			kΩ
Conversion speed	Update rate	I to i+1LSB, CLOAD=50pF				200K	Hz
Start-up time	T_{ST}			-	-	10	us
Output impedance	Rout	Buffer off		-	12.5	15	KΩ

Remark: This specification is guaranteed by the design, and is not tested in mass production

7.8.4 Comparator

(Unless otherwise specified , T_A=25℃, V_{DD}=5V, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
operating current	I_{VDD}	T_A= -40~125℃	50	120	200	uA
Turn-off current	I_{SD}	T_A= -40~125℃	-	0.01	0.6	uA
Input offset voltage	V_{OFFSET}	-	-	±6		mV
Input voltage range	V_{IN}	-	0	-	V_{DD}	V
Hysteresis voltage	V_{HYS}			±20 ±40 ±60		mV
Response time	T_{CR}, T_{CF}	Input Vip=Vin±100mV	-	50	100	ns
Running stability time	T_{STB}	-	-	-	2	us

Remark: This specification is guaranteed by the design, and is not tested in mass production.

7.8.5 Programmable gain amplifier (PGA)

(Unless otherwise specified , T_A=25℃, V_{DD}=5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
operating current	I_{VDD}	T_A= -40~125℃		0.5	0.9	1.4	mA
Turn-off current	I_{SD}	T_A= -40~125℃		-	0.01	1.2	uA
Input deviation voltage	V_{IOPGA}	G=8		-	±3	±10	mV
Input voltage range	V_{IPGA}	-		0	-	V_{DD}-1.3	V
Output voltage range	V_{IOHPGA}	-		0.3	-	-	V
	V_{IOLPGA}	-		-	-	V_{DD}-0.3	V
Gain deviation	EG	x1~x8	-	-	±3	-	%
		x10~x32	-	-	±5	-	%
Conversion rate[Note2]	SR_{RPGA}	Rising Vip-Vin=0V to1 V	G=1	7	-	-	V/us
			G=4	10	-	-	
	SR_{FPGA}	Falling Vip-Vin=1V to0 V	G=1	7	-	-	
			G=4	10	-	-	
Unit-gain bandwidth	BW	G=1, load RC=10kΩ/1uF		5			MHz
Carrying capacity	I_{LOAD}					2	mA
Stable operation time[Note1]	T_{PGA}		-	-	-	10	us
Working current	I_{PGADD}	Refer to 7.5.2 Power supply current characteristics					

Note 1: The time required from PGA action enable (PGAEN=1) to fulfill each of the PGA's DC and AC pattern requirements.

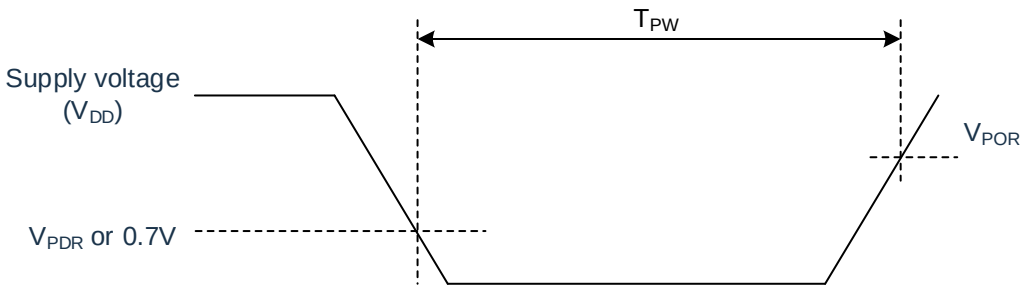
Note 2: This specification is guaranteed by the design, and is not tested in mass production.

7.8.6 POR circuit characteristics

(T_A= -40~125℃, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detect voltage	V_{POR}	When the supply voltage rises	-	1.50	2.0	V
	V_{PDR}	When the supply voltage drops	1.37	1.45	-	V
Minimum pulse width Note1	T_{PW}	-	300	-	-	us

Note 1: This is the time required to reset the POR when Vcap falls below V_{PDR}. In addition, when the oscillation of the main system clock (F_{MAIN}) is stopped by setting bit0 (HIOSTOP) and bit7 (MSTOP) of the clock operation status control register (CSC) in the deep sleep mode, this is the time required for POR reset from the time when Vcap is lower than 0.7V to the time when it rises above V_{POR}.



Remark: This specification is guaranteed by the design, and is not tested in mass production.

7.8.7 LVD circuit characteristics

(1) Reset mode, interrupt mode

(T_A= -40~125℃, V_{PDR}≤Vcap≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection voltage	V_{LVD0}	When the supply voltage rises	-	4.06	4.26	V
		When the supply voltage drops	3.78	3.98	-	V
	V_{LVD1}	When the supply voltage rises	-	3.75	-	V
		When the supply voltage drops	-	3.67	-	V
	V_{LVD2}	When the supply voltage rises	-	3.02	-	V
		When the supply voltage drops	-	2.96	-	V
	V_{LVD3}	When the supply voltage rises	-	2.71	-	V
		When the supply voltage drops	-	2.65	-	V
	V_{LVD4}	When the supply voltage rises	-	2.09	2.16	V
		When the supply voltage drops	1.97	2.04	-	V
Minimum pulse width	T_{LW}	-	300	-	-	us
Detection delay	-	-	-	-	300	us

Remark: This specification is guaranteed by the design, and is not tested in mass production.

(2) Interrupt & reset mode

(T_A= -40~125℃, V_{PDR} ≤Vcap≤5.5V, V_{SS}=0V)

Item	Symbol	Condition			Min.	Typ.	Max.	Unit
Interrupt & reset mode	V_{LVDB0}	V_{POC2}=0 V_{POC1}=0 V_{POC0}=1	Drop the reset voltage		1.78	1.84	-	V
	V_{LVDB2}		LVIS1=0 LVIS0=1	Rise the reset release voltage	-	2.09	2.16	V
				Drop the interrupt voltage	1.97	2.04	-	V
	V_{LVDC0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=0	Drop the reset voltage		-	2.45	-	V
	V_{LVDC2}		LVIS1=0 LVIS0=1	Rise the reset release voltage	-	2.71	-	V
				Drop the interrupt voltage	-	2.65	-	V
	V_{LVDC3}		LVIS1=0 LVIS0=0	Rise the reset release voltage	-	3.75	-	V
				Drop the interrupt voltage	-	3.67	-	V
	V_{LVcap0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=1	Drop the reset voltage		--	2.75	-	V
	V_{LVcap2}		LVIS1=0 LVIS0=1	Rise the reset release voltage	-	3.02		V
				Drop the interrupt voltage	-	2.96		V
	V_{LVcap3}		LVIS1=0 LVIS0=0	Rise the reset release voltage	-	4.06	4.26	V
				Drop the interrupt voltage	3.78	3.98	-	V

Remark: This specification is guaranteed by the design, and is not tested in mass production.

7.8.8 Rise slope characteristics of reset time and supply voltage

(T_A= -40~125℃, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time	T_{RESET}	-	-	1	-	ms
Rising slope of supply voltage	S_{Vcap}	-	-	-	54	V/ms

Remark: This specification is guaranteed by the design, and is not tested in mass production.

7.9 LIN transceiver characteristics

7.9.1 Limit parameters

Item	Symbol	Test condition	Value	Unit
Supply Voltage	V_{BAT}	Ground potential	-0.3 ~ +40	V
pin voltage	V_{CC}	Ground potential	-0.3~ +7	V
	V_{RXD}	Ground potential	-0.3~V_{CC}+0.3	V
	V_{EN}	Ground potential	-0.3~V_{CC}+0.3	V
	V_{RSTN}	Ground potential	-0.3~V_{CC}+0.3	V
	V_{TXD}	Ground potential	-0.3~V_{CC}+0.3	V
	V_{LIN}	Ground-to-VBAT potential	-40~ +40	V
Junction temperature	T_j	-	-40 ~ 150	℃
Storage temperature	T_{stg}	-	-55 ~ 150	℃

Notice: The Maximum Limit Parameter value means that exceeding this value may cause irrecoverable damage to the device. Such conditions are not conducive to proper device operation. Continuous operation of the device at the maximum allowable ratings may affect the reliability of the device. The reference point for all voltages is ground.

7.9.2 DC characteristics

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Power consumption						
Current consumption on the V_{BAT} pin	I_{BAT}	Sleep mode: (V_{LIN}=V_{BAT})	-	10	-	μA
		Standby mode: (V_{LIN}=V_{BAT})	-	40	-	μA
		Normal mode (recessive): (V_{LIN}=V_{BAT}; V_{TXD}=V_{CC}; V_{RSTN}=HIGH)	-	200	-	μA
		Normal mode (dominant): (V_{BAT}=12V; V_{TXD}=0V; V_{RSTN}=HIGH)	-	2.5	-	mA
Power-on reset						
V_{BAT} power-down threshold voltage	$V_{th(BAT)L}$	-	3	-	4.7	V
V_{BAT} power-up threshold voltage	$V_{th(BAT)H}$	-	-	-	5.25	V
V_{BAT} hysteresis voltage	$V_{hys(BAT)}$	-	50	-	-	V
V_{CC} pin						
Voltage regulator output voltage	V_{CC}	$V_{CC(nom)}$ =5V; I_{CC}=-70mA~0	4.9	5	5.1	V
Voltage regulator output current limit	I_{Olim}	V_{CC}=0 ~ 5.5V	-250	-	-70	mA
Power-down detection voltage	V_{UVD}	$V_{CC(nom)}$ =5V	4.2	-	4.6	V
Brown-out recovery voltage	V_{UVR}	$V_{CC(nom)}$=5V	4.6	-	4.9	V
V_{BAT} to V_{CC} resisitance	$R_{(VBAT-VCC)}$ [1]	$V_{CC(nom)}$ = 5 V; V_{BAT}= 4.5V~ 5.5V I_{V1}= -70 mA~ -5mA	-	-	5	Ω
Output capacitance	C_O [1]	ESR < 5Ω	2.2	10	-	μF
TXD pin						
Input threshold voltage	$V_{th(SW)}$	V_{CC} = 2.97V~5.5V	0.3V_{CC}	-	0.7V_{CC}	V
Input hysteresis voltage	$V_{hys(i)}$	V_{CC} = 2.97V~5.5V	200	-	-	mV
Pull-up resistance	R_{pu}	-	5	12	25	kΩ
RXD pin						
High-level output current	I_{OH}	Normal mode; V_{LIN} = V_{BAT}; V_{RXD} = V_{CC}- 0.4 V	-	-	-0.4	mA
Low-level output current	I_{OL}	Normal mode; V_{LIN} = 0; V_{RXD} = 0.4 V	0.4	-	-	mA
EN pin						
Input threshold voltage	$V_{th(SW)}$	-	0.8	-	2	V
Pull-down resistance	R_{pd}	-	50	130	400	KΩ
RSTN pin						
Pull-up resistance	R_{pu}	V_{RSTN}=V_{CC}-0.4V	3	-	12	kΩ

		V_{CC}=2.97V~5.5V				
Low-level output current	I_{OL}	V_{RSTN}=0.4V V_{CC} =2.97V~5.5V -40℃<Tj<195℃	3.2	-	40	mA
Low-level output voltage	V_{OL}	V_{CC}=2.5V~5.5 V -40℃<Tj<195℃	0	-	0.5	V
High-level output voltage	V_{OH}	-40℃<Tj<195℃	0.8V_{CC}	-	V_{CC}+0.3	V
LIN pin						
Driver dominant current limit	I_{BUS_LIM}	V_{TXD}=0V; V_{LIN}=V_{BAT}=18V	40	-	100	mA
Receiver recessive input leakage current	$I_{BUS\_PAS\_rec}$	V_{TXD}=V_{CC}; V_{LIN}=18V; V_{BAT}=5.5V	-	-	20	μA
Receiver dominant input leakage current	$I_{BUS\_PAS\_dom}$	Normal mode: V_{TXD}=V_{CC}; V_{LIN}=0V; V_{BAT}=12V	-1000	-	-	μA
Bus-to-ground leakage current	$IL_{(log)}$	V_{BAT}=18V; VLIN=0V	-1000	-	10	μA
Bus-to-supply leakage current	$IL_{(lob)}$	V_{BAT}=0V; VLIN=18V	-	-	20	μA
Receiver dominant toggle threshold voltage	$V_{th(dom)RX}$	V_{BAT}=5.5V~18V	-	-	0.4V_{BAT}	V
Receiver recessive toggle threshold voltage	$V_{th(rec)RX}$	V_{BAT}=5.5V~18V	0.6V_{BAT}	-	-	V
Receiver center toggle threshold voltage	$V_{th(RX)cntr}$	V_{BAT}=5.5V~18V $V_{th(RX)\ cntr}$= ($V_{th(rec)RX}$ + $V_{th(dom)RX}$)/2	0.475V_{BAT}	0.5V_{BAT}	0.525V_{BAT}	V
Receiver hysteresis threshold voltage	$V_{th(hys)RX}$	V_{BAT}=5.5V~18V $V_{th(hys)RX}$ =$V_{th(rec)RX}$ – $V_{th(dom)RX}$	-	-	0.175V_{BAT}	V
Slave eesistance	R_{slave}	Equivalent resistance between LIN and VBAT; V_{LIN} = 0V; V_{BAT}=12V	20	30	60	KΩ
LIN pin equivalent capacitance	C_{LIN} [1]	-	-	-	30	pF
Dominant output voltage	$V_{o(dom)}$	Normal mode; V_{TXD}=0V; V_{BAT}=7V	-	-	1.4	V
		Normal mode; V_{TXD}=0V; V_{BAT}=18V	-	-	2.0	V
Thermal shutdown						
Shutdown junction temperature	$T_{j(sd)}$ [1]	-	150	180	200	℃

(If not otherwise specified, 5.5V≤V_{BAT}≤28V, -40°C≤T_j≤150°C, typical at V_{BAT}=13V, T_j=25°C.)

[1] Values are guaranteed by design, not test results.

7.9.3 Switching characteristics

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Duty cycle						
Duty cycle 1	δ1 [1][2]	Vth(rec)(max)=0.744×VBAT; Vth(dom)(max)=0.581×VBAT; t_{bit}=50μs; V_{BAT}=7V~18V	0.396	-	-	-
		Vth(rec)(max)=0.76×VBAT; Vth(dom)(max)=0.593×VBAT; t_{bit}=50μs; V_{BAT}=5.5V~7V	0.396	-	-	-
Duty cycle 2	δ2 [2][3]	Vth(rec)(min)=0.422×VBAT; Vth(dom)(min)=0.284×VBAT; t_{bit}=50μs; V_{BAT}=7.6V~18V	-	-	0.581	-
		Vth(rec)(min)=0.41×VBAT; Vth(dom)(min)=0.275×VBAT; t_{bit}=50μs; V_{BAT}=6.1V~7.6V	-	-	0.581	-
Duty cycle 3	δ3 [1][2]	Vth(rec)(max)=0.778×VBAT; Vth(dom)(max)=0.616×VBAT; t_{bit}=96μs; V_{BAT}=7V~18V	0.417	-	-	-
		Vth(rec)(max)=0.797×VBAT; Vth(dom)(max)=0.630×VBAT; t_{bit}=96μs; V_{BAT}=5.5V~7V	0.417	-	-	-
Duty cycle 4	δ4 [2][3]	Vth(rec)(min)=0.389×VBAT; Vth(dom)(min)=0.251×VBAT; t_{bit}=96μs; V_{BAT}=7.6V~18V	-	-	0.590	-
		Vth(rec)(min)=0.378×VBAT; Vth(dom)(min)=0.242×VBAT; t_{bit}=96μs; V_{BAT}=6.1V~7.6V	-	-	0.590	-
Timing characteristics						
Receiver propagation delay	$t_{PD(RX)}$ [4]	-	-	-	6	μs
Receiver propagation delay symmetry	$t_{PD(RX)sym}$ [4]	-	-2	-	2	μs
LIN dominant wake-up time (remote wake-up)	$t_{wake(dom)LIN}$	Sleep mode	30	65	150	μs
WAKE_N dominant wake-up time (local wake-up)	$t_{wake(dom)WAKE\_N}$	Sleep mode	7	22	50	μs
Time to enter normal mode	$t_{gotonorm}$	-	2	5	10	μs
Time to enter sleep mode	$t_{gotosleep}$	-	2	5	10	μs
TXD dominant time-out time	$t_{to(dom)TXD}$	V_{TXD}=0V	27	52	90	ms

(If not otherwise specified, 5.5V≤V_{BAT}≤27V, -40°C≤T_{vj}≤150°C, typical at V_{BAT}=12V, T_{vj}=25°C.)

1) δ1, δ3=$\frac{t_{bus(rec)(min)}}{2\times t_{bit}}$

2) Bus Load: (1) C_L=1nF, R_L=1kΩ; (2) C_L=6.8nF, R_L=660Ω; (3) C_L=10nF, R_L=500Ω

3) δ2, δ4=$\frac{t_{bus(rec)(max)}}{2\times t_{bit}}$

4) Receiver output pin RXD Load condition: C_{TXD}=20pF, R_{RXD}=2.4kΩ

7.10 Memory characteristics

7.10.1 Flash memory

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Symbol	Item	Condition	Min.	Max.	Unit
T_{PROG}	Word write time (32bit)	T_A= -40~125℃	24	30	us
T_{ERASE}	Sector erase time (512B)	T_A= -40~125℃	4	5	ms
	Chip erase time	T_A= -40~125℃	20	40	ms
N_{END}	Number of rewritable times	T_A= -40~125℃	20,000	-	cycles
T_{RET}	Data retention period	T_A =125℃	20	-	years

Remark: This specification is guaranteed by the design, and is not tested in mass production.

7.10.2 RAM memory

(T_A= -40~125℃, 2.0V≤Vcap≤5.5V, V_{SS}=GND=0V)

Symbol	Item	Condition	Min.	Max.	Unit
$V_{RAMHOLD}$	RAM hold voltage	T_A= -40~125℃	0.8	-	V

Remark: This specification is guaranteed by the design, and is not tested in mass production.

7.11 EMS characteristics

7.11.1 ESD electrical characteristics

Symbol	Item	Test condition	Grade
$V_{ESD(HBM)}$	Electrostatic discharge (Human-Body Model HBM)	AEC-Q100-002 Rev-E: 2013	3A

Remark: This specification is guaranteed by the design, and is not tested in mass production.

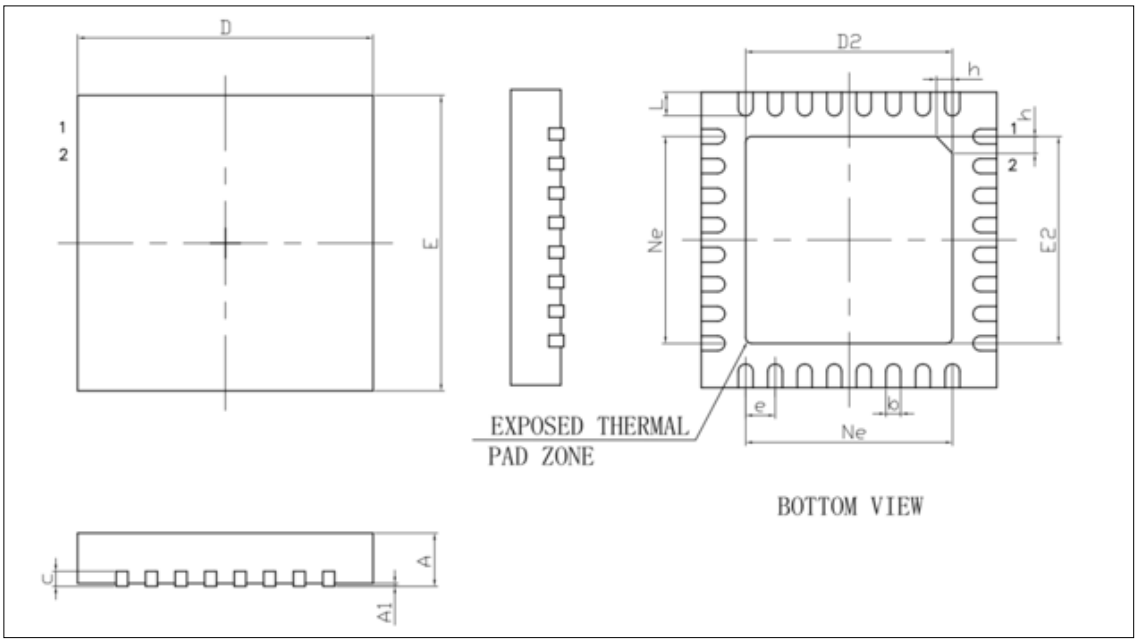
7.11.2 Latch-up electrical characteristics

Symbol	Item	Test condition	Classification
LU	Static latch-up class	AEC-Q100-004 Rev-D: 2012	IIA

Remark: This specification is guaranteed by the design, and is not tested in mass production.

8 Package

8.1 QFN32 (5x5mm, 0.5mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F carrier dimensions	150*150		130*130

Caution: Package dimensions do not include mold flash or gate burrs.

9 Revision History

Version	Date	Revised content
V0.0.1	May 2023	Initial version
V0.0.2	August 2023	1) Corrected the content of the functional description. 2) Revised description of Section 1.1. 3) Modified memory mapping in Chapter 4. 4) Modified functional description of Sections 5.1/5.1.1/5.2. 5) Revised Chapters 6.2.1/6.2.2/6.7.1/6.21/6.22/6.23. 6) Added Chapter LIN/UART module (LIN). 7) Corrected electrical parameters of Sections 7.2/7.9.2.
V0.0.3	September 2023	1) Changed the way of describing relevant electrical characteristics. 2) Added Section: 6.4 LIN transceiver.
V0.1.0	October 2023	1) Updated descriptions of Sections 6.1/6.24. 2) Updated parameters for Section 7.6.
V0.1.1	October 2023	1) Updated parameters for Section 7.9.2 2) Corrected content in 6.5 Linkage controller and Functions
V0.5.0	November 2023	1) Updated TBD parameters in the manual 2) Add some parameters in Section 7.2 and 7.5.2
V0.5.1	November 2023	1) Updated parameters in section 7.5.1 and 7.5.2 2) Updated 7.10.1Times of Flash Erase 3) Corrects function section content
V0.5.2	December 2023	1) Modify 5.1.1 Pin description 2) Added Section: 5.3 3) Updated parameters in section 7.5.2
V0.5.3	April 2024	1) Modified section 7.1 Typical application peripheral circuits 2) Add input current parameters in section 7.3 3) Modify the Vcap function description
V0.5.4	April 2024	Corrected Section 2 Product Structure Diagram
V0.5.5	July 2024	1) Correct the data in the section 7.5.2 2) Modify 7.2/7.3/7.4.1/7.4.2/7.5.2/7.8.2/7.8.3 production test related note 3) Remove the TBD data from the section 7.8.3 4) Update QFN32 encapsulation information 5) Modify the EMS characteristics